## General Description

The MAX8610-MAX8613/MAX8611V are highly efficient complete power-supply solutions for digital still cameras (DSCs) and digital video cameras (DVCs). Seven internal-MOSFET DC-DC converters provide up to 95\% efficiency and generate all critical power supplies in DSC systems. They also feature True Shutdown ${ }^{\text {TM }}$, as well as internal compensation to minimize external component count. One additional converter operates with an external MOSFET for optimum design flexibility. In all, eight converter channels include:

- Synchronous-rectified step-up with True Shutdown.
- Two synchronous-rectified step-down (MAX8611/ MAX8613/MAX8611V) or step-up (MAX8610/ MAX8612) converters power DSC system, I/O, and AFE blocks.
- Low-Vout (down to 1V), synchronous-rectified step-down to power a DSP core.
- High-output-voltage step-up for CCD bias.
- Transformerless inverter for negative CCD bias.
- High-output-voltage step-up for white LEDs, OLED display, or other output.
- Auxiliary DC-DC boost (MAX8611/MAX8610/ MAX8611V) or inverting (MAX8612/MAX8613) controller.
The MAX8611/MAX8613/MAX8611V operate in 1-cell lithium-ion (Li+) and dual-battery ( $\mathrm{Li}+$ and 2 AA ) designs. The MAX8610/MAX8612 operate in 2 AA designs.

| Applications |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| DSCs and DVCs $\quad$ PDAs and MP3 Players |  |  |  |  |  |  |  |

True Shutdown is a trademark of Maxim Integrated Products, Inc.
Typical Operating Circuit


Features

- 95\% Efficient Synchronous-Rectified DC-DCs
- 90\% Efficient Boost-Buck Operation
- 85\% Efficient DC-DCs for CCD, LCD, WLED, and/or OLED
- Auxiliary Power for Motors
(MAX8610/MAX8611/MAX8611V)
- Internal Compensation
- True Shutdown Step-Up Converters
- Overload Protection
- Soft-Start for Controlled Startup Current
- Low-Dropout (100\% Duty Cycle) Step-Downs
- Regulated Current for Up to 6 White LEDS
- Open-LED Overvoltage Protection
- Transformerless Inverting Converter for CCD
- Adjustable 1MHz to 2MHz Switching Frequency
- 3\% Frequency Accuracy
- 1 $\mu \mathrm{A}$ Shutdown Supply Current
- CCD Voltage Sequencing
- Voltage Tracking for Core and Logic (MAX8611/MAX8613/MAX8611V)
- Compact 48 -Pin, $6 \mathrm{~mm} \times 6 \mathrm{~mm}$ Thin QFN Package

Ordering Information

| PART | TEMP RANGE | PIN- <br> PACKAGE | PKG <br> CODE |
| :---: | :---: | :--- | :---: |
| MAX8610ETM + | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | $48 \mathrm{TQFN}-\mathrm{EP}^{\star}$ <br> $6 \mathrm{~mm} \times 6 \mathrm{~mm}$ | T4866-1 |
| MAX8611ETM + | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | $48 \mathrm{TQFN}-\mathrm{EP}^{\star}$ <br> $6 \mathrm{~mm} \times 6 \mathrm{~mm}$ | T4866-1 |
| MAX8611VETM $+-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | $48 \mathrm{TQFN}-\mathrm{EP*}$ <br> $6 \mathrm{~mm} \times 6 \mathrm{~mm}$ | T4866-1 |  |
| MAX8612ETM + | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | $48 \mathrm{TQFN}-\mathrm{EP*}$ <br> $6 \mathrm{~mm} \times 6 \mathrm{~mm}$ | T4866-1 |
| MAX8613ETM + | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | $48 \mathrm{TQFN}-\mathrm{EP}^{\star}$ <br> $6 \mathrm{~mm} \times 6 \mathrm{~mm}$ | T4866-1 |

*EP = Exposed paddle.
+Denotes lead-free package.

Selector Guide and Pin Configuration appear at end of data sheet.

## 8-Channel PMICs for Digital Camera Power Supplies

## ABSOLUTE MAXIMUM RATINGS



CCAUX to GND .....................-0.3V to max (BATT, PVSU) + 0.3V Continuous Power Dissipation $\left(\mathrm{T}_{\mathrm{A}}=+70^{\circ} \mathrm{C}\right)$

48 -Pin TQFN $6 \mathrm{~mm} \times 6 \mathrm{~mm} . . . . . . .2105 \mathrm{~mW}$ (single-layer board) 48-Pin TQFN $6 \mathrm{~mm} \times 6 \mathrm{~mm} . . . . . . . . . . .2963 \mathrm{~mW}$ (multilayer board) Operating Temperature Range . ...................... $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ Junction Temperature $+150^{\circ} \mathrm{C}$ Storage Temperature Range ............................. $-65^{\circ} \mathrm{C}$ to $+165^{\circ} \mathrm{C}$ Lead Temperature (soldering, 10s)

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
Note 1: For step-up converters (SU and MAIN/AFE (MAX8610/MAX8612)), LX_ has internal clamp diodes to the IC internal power node, VPWR (where VPWR is the higher of BATT or PVSU), and PG_. For step-down converters (MAIN/AFE (MAX8611/ MAX8613/MAX8611V) and SD)), LX_ has internal clamp diodes to $\overline{P V}$ _ and PG_. Applications that forward bias these diodes should take care not to exceed the devices' power dissipation limits.

## ELECTRICAL CHARACTERISTICS

(BATT $=$ PVINV $=$ PVLED $=$ PVBST $=P V S D=P V M=P V A F E=3.6 V, P V S U=S U=5 V, G N D=P G S U=P G M=P G A F E=P G S D=$ PG1 $=\mathrm{PG} 2=0 \mathrm{~V}, \mathrm{CREF}=0.22 \mu \mathrm{~F}, \mathrm{RREXT}=100 \mathrm{k} \Omega$ to $\mathrm{GND}, \mathbf{T}_{\mathbf{A}}=\mathbf{0}^{\circ} \mathbf{C}$ to $+\mathbf{8 5} 5^{\circ} \mathbf{C}$, unless otherwise noted. Typical values are at $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$.)

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
| :---: | :---: | :---: | :---: | :---: | :---: |
| GENERAL |  |  |  |  |  |
| Input Voltage Range | (Note 1) | 0.9 |  | 5.5 | V |
| Minimum SU Startup Voltage |  |  | 1.2 | 1.5 | V |
| SU Step-Up Startup Frequency |  |  | 2 |  | MHz |
| Shutdown Supply Current | $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ |  | 0.1 | 10 | $\mu \mathrm{A}$ |
|  | $\mathrm{T}_{\mathrm{A}}=+85^{\circ} \mathrm{C}$ |  | 0.1 |  |  |
| Supply Current with SU Step-Up Enabled | ONSU $=3.6 \mathrm{~V}$, IBATT + ISU (does not include switching losses) |  | 510 | 700 | $\mu \mathrm{A}$ |
| Supply Current with SU Step-Up and SD Step-Down Enabled | ONSU = ONSD $=3.6 \mathrm{~V}$, IBATT + ISU (does not include switching losses) |  | 550 | 775 | $\mu \mathrm{A}$ |
| Supply Current with SU Step-Up and MAIN Enabled | ONSU = ONM = 3.6V, IBATT + ISU (does not include switching losses) |  | 550 | 775 | $\mu \mathrm{A}$ |
| Supply Current with SU Step-Up and AFE Enabled | ONSU = ONAFE $=3.6 \mathrm{~V}$, IBATT + ISU (does not include switching losses) |  | 550 | 775 | $\mu \mathrm{A}$ |
| Supply Current with SU Step-Up and LED Enabled | ONSU = ONLED $=3.6 \mathrm{~V}$, IBATT + ISU (does not include switching losses) |  | 600 | 875 | $\mu \mathrm{A}$ |
| Supply Current with SU Step-Up and CCD BST Enabled | ONSU = ONBST $=3.6 \mathrm{~V}$, SEQCCD $=$ GND, IBATT +ISU (does not include switching losses) |  | 560 | 875 | $\mu \mathrm{A}$ |
| Supply Current with SU Step-Up and CCD INV Enabled | ONSU = ONINV = 3.6V, SEQCCD = GND, IBATT + ISU (does not include switching losses) |  | 560 | 775 | $\mu \mathrm{A}$ |
| Supply Current with SU Step-Up and AUX Enabled | ONSU = ONAUX = 3.6V, IBATT + ISU (does not include switching losses) |  | 615 | 875 | $\mu \mathrm{A}$ |
| REFERENCE (REF) |  |  |  |  |  |
| Reference Output Voltage | $I_{\text {REF }}=20 \mu \mathrm{~A}$ | 1.24 | 1.25 | 1.26 | V |
| Reference Load Regulation | $10 \mu \mathrm{~A}$ < IREF < 100 $\mu \mathrm{A}$ |  | 3 | 10 | mV |
| Reference Line Regulation | $3.3 \mathrm{~V}<\mathrm{PVSU}=\mathrm{SU}<5.5 \mathrm{~V}$ |  | 0 | 5 | mV |

# 8-Channel PMICs for Digital Camera Power Supplies 

## ELECTRICAL CHARACTERISTICS (continued)

(BATT $=\mathrm{PVINV}=\mathrm{PVLED}=\mathrm{PVBST}=\mathrm{PVSD}=\mathrm{PVM}=\mathrm{PVAFE}=3.6 \mathrm{~V}, \mathrm{PVSU}=\mathrm{SU}=5 \mathrm{~V}, \mathrm{GND}=\mathrm{PGSU}=\mathrm{PGM}=\mathrm{PGAFE}=\mathrm{PGSD}=$ PG1 $=\mathrm{PG} 2=0 \mathrm{~V}, \mathrm{C}_{\text {REF }}=0.22 \mu \mathrm{~F}, \mathrm{RREXT}=100 \mathrm{k} \Omega$ to $\mathrm{GND}, \mathbf{T}_{\mathbf{A}}=\mathbf{0}^{\circ} \mathbf{C}$ to $+\mathbf{8 5} 5^{\circ} \mathbf{C}$, unless otherwise noted. Typical values are at $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$.)


Idle Mode is a trademark of Maxim Integrated Products, Inc.

## 8-Channel PMICs for Digital Camera Power Supplies

## ELECTRICAL CHARACTERISTICS (continued)

(BATT $=$ PVINV $=$ PVLED $=$ PVBST $=P V S D=P V M=P V A F E=3.6 V, P V S U=S U=5 V$, GND $=P G S U=P G M=P G A F E=P G S D=$ PG1 $=\mathrm{PG} 2=0 \mathrm{~V}, \mathrm{C}_{\text {REF }}=0.22 \mu \mathrm{~F}, \mathrm{R}$ REXT $=100 \mathrm{k} \Omega$ to $\mathrm{GND}, \mathbf{T}_{\mathbf{A}}=\mathbf{0}^{\circ} \mathbf{C}$ to $+\mathbf{8 5} \mathbf{5}^{\circ} \mathbf{C}$, unless otherwise noted. Typical values are at $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$.)

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
| :--- | :--- | ---: | ---: | :---: | :---: |
| LX_ Leakage Current | $\mathrm{LX}=\mathrm{OV}, 3.6 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ | -5 | +0.1 | +5 | $\mu \mathrm{~A}$ |
|  | $\mathrm{LX}=0 \mathrm{~V}, 3.6 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+85^{\circ} \mathrm{C}$ | 0.1 |  |  |  |
| n-Channel On-Resistance |  | 0.1 | 0.175 | $\Omega$ |  |
| p-Channel On-Resistance |  | 0.14 | 0.25 | $\Omega$ |  |
| n-Channel Current Limit |  | 2.25 | 2.5 | 2.75 | A |
| p-Channel Turn-Off Current |  | 10 | mA |  |  |
| Soft-Start Interval |  | 15,000 | OSC <br> cycles |  |  |
| Overload Protection Fault Delay |  | 200,000 | OSC <br> cycles |  |  |

MAIN/AFE STEP-DOWN DC-DC CONVERTER (MAX8611/MAX8613/MAX8611V)

| Step-Down Voltage Adjust Range |  |  | 1 |  | SU | V |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| FB_Regulation Voltage | No load |  | 0.995 | 1.01 | 1.025 | V |
| FB_Load Regulation |  |  | -20 |  |  | $\mathrm{mV} / \mathrm{A}$ |
| FB_Line Regulation |  |  | -10 |  |  | mV/D |
| FB_ Input Leakage Current | FB_= $1.01 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ |  | -50 | -5 | +50 | nA |
|  | FB_= $1.01 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+85^{\circ} \mathrm{C}$ |  | -5 |  |  |  |
| Idle-Mode Trip Level | (Note 2) | MAX8611/MAX8613 | 50 |  |  | mA |
|  |  | MAX8611V | 125 |  |  |  |
| LX_ Leakage Current | LX - $=0 \mathrm{~V}, 3.6 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ |  | -5 | +0.1 | +5 | $\mu \mathrm{A}$ |
|  | $L X=0 \mathrm{~V}, 3.6 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+85^{\circ} \mathrm{C}$ |  | 0.1 |  |  |  |
| n-Channel On-Resistance |  |  |  | 0.1 | 0.175 | $\Omega$ |
| p-Channel On-Resistance |  |  |  | 0.14 | 0.25 | $\Omega$ |
| p-Channel Current Limit |  |  | 0.9 | 1 | 1.1 | A |
| n-Channel Turn-Off Current |  |  |  | 10 |  | mA |
| Soft-Start Interval |  |  |  | 15,000 |  | OSC <br> cycles |
| Overload Protection Fault Delay |  |  |  | 200,000 |  | $\begin{gathered} \text { OSC } \\ \text { cycles } \end{gathered}$ |
| SD STEP-DOWN DC-DC CONVER | TER |  |  |  |  |  |
| SD Step-Down Voltage Adjust Range |  |  | 1 |  | SU | V |
| FBSD Regulation Voltage | No load |  | 0.995 | 1.01 | 1.025 | V |
| FBSD Load Regulation |  |  |  | -20 |  | mV/A |
| FBSD Line Regulation |  |  |  | -10 |  | mV/D |
| FBSD Input Leak | FBSD $=1$. |  | -50 | -5 | +50 |  |
| FBSD Input Leakage Current | FBSD $=$ |  |  | -5 |  |  |
| Ido-Mode Trip Level |  | MAX8610-MAX8613 |  | 50 |  |  |
| Idle-Mode Trip Level | (Note 2) | MAX8611V |  | 125 |  | mA |

## 8-Channel PMICs for Digital Camera Power Supplies

## ELECTRICAL CHARACTERISTICS (continued)

(BATT $=$ PVINV $=$ PVLED $=$ PVBST $=\mathrm{PVSD}=\mathrm{PVM}=\mathrm{PVAFE}=3.6 \mathrm{~V}, \mathrm{PVSU}=\mathrm{SU}=5 \mathrm{~V}, \mathrm{GND}=\mathrm{PGSU}=\mathrm{PGM}=\mathrm{PGAFE}=\mathrm{PGSD}=$ PG1 $=P G 2=0 V, C_{\text {REF }}=0.22 \mu F$, RREXT $=100 \mathrm{k} \Omega$ to $G N D, \mathbf{T}_{\mathbf{A}}=\mathbf{0}^{\circ} \mathbf{C}$ to $+\mathbf{8 5} 5^{\circ} \mathbf{C}$, unless otherwise noted. Typical values are at $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$.)

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
| :---: | :---: | :---: | :---: | :---: | :---: |
| LXSD Leakage Current | LXSD $=0 \mathrm{~V}, 3.6 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ | -5 | +0.1 | +5 | $\mu \mathrm{A}$ |
|  | LXSD $=0 \mathrm{~V}, 3.6 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+85^{\circ} \mathrm{C}$ | +0.1 |  |  |  |
| n-Channel On-Resistance |  |  | 0.1 | 0.175 | $\Omega$ |
| p-Channel On-Resistance |  |  | 0.14 | 0.25 | $\Omega$ |
| p-Channel Current Limit |  | 0.9 | 1.0 | 1.1 | A |
| n-Channel Turn-Off Current |  |  | 10 |  | mA |
| Soft-Start Interval |  |  | 5000 |  | $\begin{gathered} \text { OSC } \\ \text { cycles } \end{gathered}$ |
| Overload Protection Fault Delay |  |  | 200,000 |  | $\begin{gathered} \text { OSC } \\ \text { cycles } \end{gathered}$ |
| CCD BST DC-DC CONVERTER |  |  |  |  |  |
| BST Voltage Adjust Range |  | BATT |  | 27 | V |
| FBBST Regulation Voltage | No load | 0.995 | 1.01 | 1.025 | V |
| FBBST Load Regulation |  |  | -15 |  | mV/A |
| FBBST Line Regulation |  |  | -20 |  | mV/D |
| FBBST Input Leakage Current | FBBST $=1.01 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ | -50 | -5 | +50 | nA |
|  | FBBST $=1.01 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+85^{\circ} \mathrm{C}$ |  | -5 |  |  |
| SWBST Leakage Current | SWBST $=0 \mathrm{~V}, \mathrm{PVBST}=3.6 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ | -5 | +0.1 | +5 | $\mu \mathrm{A}$ |
|  | SWBST $=0 \mathrm{~V}, \mathrm{PVBST}=3.6 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+85^{\circ} \mathrm{C}$ |  | 0.1 |  |  |
| LXBST Leakage Current | LXBST $=26 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ | -5 | +0.1 | +5 | $\mu \mathrm{A}$ |
|  | LXBST $=26 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+85^{\circ} \mathrm{C}$ |  | 0.1 |  |  |
| Load Switch On-Resistance |  |  | 0.09 | 0.15 | $\Omega$ |
| DMOS On-Resistance |  |  | 0.4 |  | $\Omega$ |
| SWBST Current Limit |  | 0.7 | 0.8 | 0.9 | A |
| SWBST Short-Circuit Current Limit |  | 0.95 | 1.05 | 1.15 | A |
| Soft-Start Interval |  |  | 15,000 |  | $\begin{gathered} \text { OSC } \\ \text { cycles } \end{gathered}$ |
| Overload Protection Fault Delay |  |  | 200,000 |  | OSC cycles |
| GD Leakage Current | $\mathrm{GD}=3.6 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ |  | 0.1 | 5 | $\mu \mathrm{A}$ |
|  | $\mathrm{GD}=3.6 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+85^{\circ} \mathrm{C}$ |  | 0.1 |  |  |
| CCD INV DC-DC CONVERTER |  |  |  |  |  |
| INV Voltage Adjust Range |  | $\begin{gathered} \hline \text { PVINV } \\ -16 \end{gathered}$ |  | 0 | V |
| FBINV Regulation Voltage | No load | +10 | 0 | -10 | mV |
| FBINV Load Regulation |  |  | 23 |  | $\mathrm{mV} / \mathrm{A}$ |
| FBINV Line Regulation | (Note 3) |  | 20 |  | $\begin{gathered} \mathrm{mV} / \\ (\mathrm{D}-0.5) \end{gathered}$ |

## 8-Channel PMICs for Digital Camera Power Supplies

## ELECTRICAL CHARACTERISTICS (continued)

(BATT $=$ PVINV $=$ PVLED $=$ PVBST $=P V S D=P V M=P V A F E=3.6 V, P V S U=S U=5 V$, GND $=P G S U=P G M=P G A F E=P G S D=$ PG1 $=\mathrm{PG} 2=0 \mathrm{~V}, \mathrm{C}_{\text {REF }}=0.22 \mu \mathrm{~F}, \mathrm{R}$ REXT $=100 \mathrm{k} \Omega$ to $\mathrm{GND}, \mathbf{T}_{\mathbf{A}}=\mathbf{0}^{\circ} \mathbf{C}$ to $+\mathbf{8 5} \mathbf{5}^{\circ} \mathbf{C}$, unless otherwise noted. Typical values are at $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$.)

| PARAMETER | CONDITIONS |  | MIN | TYP | MAX | UNITS |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| FBINV Input Leakage Current | $F B I N V=0 V, T_{A}=+25^{\circ} \mathrm{C}$ |  | -50 | -5 | +50 | nA |
|  | FBINV $=0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+85^{\circ} \mathrm{C}$ |  | -5 |  |  |  |
| LXINV Leakage Current | LXINV $=-12 \mathrm{~V}, \mathrm{PV}$ INV $=3.6 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ |  | -5 | +0.1 | +5 | $\mu \mathrm{A}$ |
|  | LXINV $=-12 \mathrm{~V}, \mathrm{PV}$ INV $=3.6 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+85^{\circ} \mathrm{C}$ |  | 0.1 |  |  |  |
| HVPMOS On-Resistance |  |  |  | 0.575 | 1.0 | $\Omega$ |
| HVPMOS Current Limit |  |  | 0.65 | 0.75 | 0.85 | A |
| Soft-Start Interval |  |  |  | 15,000 |  | $\begin{gathered} \text { OSC } \\ \text { cycles } \end{gathered}$ |
| Overload Protection Fault Delay |  |  |  | 200,000 |  | $\begin{aligned} & \text { OSC } \\ & \text { cycles } \end{aligned}$ |
| LED BST DC-DC CONVERTER |  |  |  |  |  |  |
| LED Voltage Adjust Range |  |  | BATT |  | 27 | V |
| FBHLED Regulation Voltage | No load, FBLED $=0 \mathrm{~V}$ |  | 1.00 | 1.015 | 1.03 | V |
| FBHLED Load Regulation |  |  | -15 |  |  | $\mathrm{mV} / \mathrm{A}$ |
| FBHLED Line Regulation |  |  | -20 |  |  | mV/D |
| FBHLED Input Leakage Current | FBHLED $=1.01 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ |  | -50 | -5 | +50 | nA |
|  | FBHLED $=1.01 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+85^{\circ} \mathrm{C}$ |  | -5 |  |  |  |
| FBLLED Regulation Voltage | No load, FBHLED $=0 \mathrm{~V}$ |  | 220 | 235 | 255 | mV |
|  |  | $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ | 225 | 235 | 245 |  |
| FBLLED Load Regulation |  |  |  | -15 |  | $\mathrm{mV} / \mathrm{A}$ |
| FBLLED Line Regulation |  |  |  | -20 |  | mV/D |
| FBLLED Input Leakage Current | FBLLED $=0.225 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ |  | -50 | -5 | +50 | nA |
|  | FBLLED $=0.225 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+85^{\circ} \mathrm{C}$ |  | -5 |  |  |  |
| SWLED Leakage Current | SWLED $=0 \mathrm{~V}, \mathrm{PVLED}=3.6 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ |  | -5 | +0.1 | +5 | $\mu \mathrm{A}$ |
|  | SWLED $=0 \mathrm{~V}, \mathrm{PVLED}=3.6 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+85^{\circ} \mathrm{C}$ |  | 0.1 |  |  |  |
| LXLED Leakage Current | LXLED $=26 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ |  | -5 | +0.1 | +5 | $\mu \mathrm{A}$ |
|  | LXLED $=26 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+85^{\circ} \mathrm{C}$ |  | 0.1 |  |  |  |
| Load Switch On-Resistance |  |  |  | 0.09 | 0.15 | $\Omega$ |
| DMOS On-Resistance |  |  | 0.4 |  |  | $\Omega$ |
| SWLED Current Limit |  |  | 0.7 | 0.8 | 0.9 | A |
| SWLED Short-Circuit Current Limit |  |  | 0.95 | 1.05 | 1.15 | A |
| Soft-Start Interval |  |  | 15,000 |  |  | $\begin{aligned} & \text { OSC } \\ & \text { cycles } \end{aligned}$ |
| Overload Protection Fault Delay |  |  | 200,000 |  |  | $\begin{gathered} \text { OSC } \\ \text { cycles } \end{gathered}$ |
| AUXILIARY CONTROLLER |  |  |  |  |  |  |
| FBAUX Regulation Voltage (MAX8610/MAX8611/MAX8611V) |  |  | 1.23 | 1.25 | 1.26 | V |

## 8-Channel PMICs for Digital Camera Power Supplies

## ELECTRICAL CHARACTERISTICS (continued)

(BATT $=\mathrm{PVINV}=\mathrm{PVLED}=\mathrm{PVBST}=\mathrm{PVSD}=\mathrm{PVM}=\mathrm{PVAFE}=3.6 \mathrm{~V}, \mathrm{PVSU}=\mathrm{SU}=5 \mathrm{~V}, \mathrm{GND}=\mathrm{PGSU}=\mathrm{PGM}=\mathrm{PGAFE}=\mathrm{PGSD}=$ PG1 $=P G 2=0 V, C_{\text {REF }}=0.22 \mu F$, RREXT $=100 \mathrm{k} \Omega$ to $G N D, \mathbf{T}_{\mathbf{A}}=\mathbf{0}^{\circ} \mathbf{C}$ to $+\mathbf{8 5} 5^{\circ} \mathbf{C}$, unless otherwise noted. Typical values are at $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$.)

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
| :---: | :---: | :---: | :---: | :---: | :---: |
| FBAUX Regulation Voltage (MAX8612/MAX8613) |  | -10 | 0 | +10 | mV |
| FBAUX Input Leakage Current | FBAUX $=1.25 \mathrm{~V}$ (MAX8610/MAX8611/MAX8611V), <br> FBAUX $=0 V\left(\right.$ MAX8612/MAX8613), $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ | -50 | -5 | +50 | nA |
|  | FBAUX $=1.25 \mathrm{~V}$ (MAX8610/MAX8611/MAX8611V), <br> FBAUX $=0 V($ MAX8612 $/ \mathrm{MAX} 8613), \mathrm{T}_{\mathrm{A}}=+85^{\circ} \mathrm{C}$ |  | -5 |  |  |
| FBAUX-CCAUX Open-Loop Voltage Gain |  |  | 80 |  | dB |
| FBAUX-CCAUX Unity-Gain Bandwidth |  |  | 3 |  | MHz |
| AUX Voltage Ramp |  |  | 1.25 |  | V |
| CCAUX Maximum Output Current | Sourcing or sinking | 90 |  |  | $\mu \mathrm{A}$ |
| DRVAUX On-Resistance | Output high or low |  | 5 | 10 | $\Omega$ |
| DRVAUX Drive Current |  |  | 0.5 |  | A |
| Soft-Start Interval |  |  | 15,000 |  | $\begin{aligned} & \text { OSC } \\ & \text { cycles } \end{aligned}$ |
| Overload Protection Fault Delay |  |  | 200,000 |  | $\begin{aligned} & \text { OSC } \\ & \text { cycles } \end{aligned}$ |
| LOGIC INPUTS |  |  |  |  |  |
| ONSU Input Low Level | 1.5 V < PVSU $=\mathrm{SU}=\mathrm{BATT}<5.5 \mathrm{~V}$ |  |  | 0.5 | V |
| ONSU Input High Level | $1.5 \mathrm{~V}<\mathrm{PVSU}=\mathrm{SU}=\mathrm{BATT}<5.5 \mathrm{~V}, \mathrm{VH}$ is higher of PVSU and BATT | VH-0.2V <br> with a <br> max of <br> 1.6V |  |  | V |
| ONM, ONAFE, ONSD, ONBST, ONINV, ONLED, ONAUX Input Low Level | $3.3 \mathrm{~V}<\mathrm{PVSU}=\mathrm{SU}=$ BATT $<5.5 \mathrm{~V}$ |  |  | 0.5 | V |
| ONM, ONAFE, ONSD, ONBST, ONINV, ONLED, ONAUX Input High Level | $3.3 \mathrm{~V}<\mathrm{PVSU}=\mathrm{SU}=\mathrm{BATT}<5.5 \mathrm{~V}$ | 1.6 |  |  | V |
| SEQCCD Input Low Level | $3.3 \mathrm{~V}<\mathrm{PVSU}=\mathrm{SU}=\mathrm{BATT}<5.5 \mathrm{~V}$ |  |  | 0.5 | V |
| SEQCCD Input High Level | $\mathrm{PVSU}=\mathrm{SU}=\mathrm{BATT}=3.3 \mathrm{~V}$ | 2.3 |  |  | V |
|  | $\mathrm{PVSU}=\mathrm{SU}=\mathrm{BATT}=5.5 \mathrm{~V}$ | 3.4 |  |  |  |
| Input Bias Current | $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ |  | 0.1 | 1 | $\mu \mathrm{A}$ |
|  | $\mathrm{T}_{\mathrm{A}}=+85^{\circ} \mathrm{C}$ |  | 0.1 |  |  |
| THERMAL LIMIT |  |  |  |  |  |
| Thermal Limit |  |  | +174 |  | ${ }^{\circ} \mathrm{C}$ |

## 8-Channel PMICs for Digital Camera Power Supplies

## ELECTRICAL CHARACTERISTICS

(BATT $=$ PVINV $=$ PVLED $=$ PVBST $=P V S D=P V M=P V A F E=3.6 V$, PVSU $=S U=5 \mathrm{~V}, \mathrm{GND}=\mathrm{PGSU}=\mathrm{PGM}=\mathrm{PGAFE}=\mathrm{PGSD}=$ PG1 $=$ PG2 $=0 \mathrm{~V}, \mathrm{C}_{\text {REF }}=0.22 \mu \mathrm{~F}$, RREXT $=100 \mathrm{k} \Omega$ to $\mathrm{GND}, \mathrm{T}_{\mathbf{A}}=\mathbf{- 4 0 ^ { \circ }} \mathbf{C}$ to $\mathbf{+ 8 5} \mathbf{\circ} \mathbf{C}$, unless otherwise noted. Specifications to $-40^{\circ} \mathrm{C}$ are guaranteed by design, not production tested.)

| PARAMETER | CONDITIONS | MIN | TYP MAX | UNITS |
| :---: | :---: | :---: | :---: | :---: |
| GENERAL |  |  |  |  |
| Input Voltage Range | (Note 1) | 0.9 | 5.5 | V |
| Minimum SU Startup Voltage |  |  | 1.5 | V |
| Supply Current with SU Step-Up Enabled | $\mathrm{ONSU}=3.6 \mathrm{~V}, \mathrm{I}$ BATT +IVSU (does not include switching losses) |  | 700 | $\mu \mathrm{A}$ |
| Supply Current with SU Step-Up and SD Step-Down Enabled | ONSU = ONSD $=3.6 \mathrm{~V}$, IBATT + IVSU (does not include switching losses) |  | 775 | $\mu \mathrm{A}$ |
| Supply Current with SU Step-Up and MAIN Enabled | ONSU = ONM = 3.6V, IBATT + Ivsu (does not include switching losses) |  | 775 | $\mu \mathrm{A}$ |
| Supply Current with SU Step-Up and AFE Enabled | ONSU = ONAFE $=3.6 \mathrm{~V}$, IbATt + IvSU (does not include switching losses) |  | 775 | $\mu \mathrm{A}$ |
| Supply Current with SU Step-Up and LED Enabled | ONSU $=$ ONLED $=3.6 \mathrm{~V}$, IBATT + IVSU (does not include switching losses) |  | 875 | $\mu \mathrm{A}$ |
| Supply Current with SU Step-Up and CCD BST Enabled | ONSU = ONBST $=3.6 \mathrm{~V}, \mathrm{SEQCCD}=\mathrm{GND}$, IBATT + IvSU (does not include switching losses) |  | 875 | $\mu \mathrm{A}$ |
| Supply Current with SU Step-Up and CCD INV Enabled | ONSU = ONINV = 3.6V, SEQCCD = GND, IBATT + ISU (does not include switching losses) |  | 775 | $\mu \mathrm{A}$ |
| Supply Current with SU Step-Up and AUX Enabled | ONSU = ONAUX = 3.6V, IBATT + ISU (does not include switching losses) |  | 875 | $\mu \mathrm{A}$ |
| REFERENCE (REF) |  |  |  |  |
| Reference Output Voltage | IREF $=20 \mu \mathrm{~A}$ | 1.24 | 1.26 | V |
| Reference Load Regulation | $10 \mu \mathrm{~A}<1 \mathrm{IREF}<100 \mu \mathrm{~A}$ |  | 10 | mV |
| Reference Line Regulation | 3.3 V < PVSU $=$ SU < 5.5V |  | 5 | mV |
| OSCILLATOR (OSC) |  |  |  |  |
| SU Step-Up/MAIN/AFE/SD Step-Down Switching Frequency | REXT $=100 \mathrm{k} \Omega$ | 1.92 | 2.08 | MHz |
| CCD/LED Switching Frequency | REXT $=100 \mathrm{k} \Omega$ | 0.96 | 1.04 | MHz |
| AUX Switching Frequency | REXT $=100 \mathrm{k} \Omega$ | 0.475 | 0.525 | MHz |
| AUX Maximum Duty Cycle | REXT $=100 \mathrm{k} \Omega$ | 86 | 89 | \% |
| SU STEP-UP DC-DC CONVERTER |  |  |  |  |
| Step-Up Voltage Adjust Range |  | 3.3 | 5.0 | V |
| FBSU Regulation Voltage | No load | 0.995 | 1.025 | V |
| n-Channel On-Resistance |  |  | 0.175 | $\Omega$ |
| p-Channel On-Resistance |  |  | 0.25 | $\Omega$ |
| n-Channel Current Limit |  | 2.25 | 2.75 | A |

## 8-Channel PMICs for Digital Camera Power Supplies

## ELECTRICAL CHARACTERISTICS (continued)

(BATT $=$ PVINV $=$ PVLED $=$ PVBST $=P V S D=P V M=P V A F E=3.6 V$, PVSU $=S U=5 \mathrm{~V}, \mathrm{GND}=\mathrm{PGSU}=\mathrm{PGM}=\mathrm{PGAFE}=\mathrm{PGSD}=$ PG1 $=\mathrm{PG} 2=0 \mathrm{~V}, \mathrm{C}_{\text {REF }}=0.22 \mu \mathrm{~F}$, RREXT $=100 \mathrm{k} \Omega$ to $\mathrm{GND}, \mathrm{T}_{\mathbf{A}}=\mathbf{- 4 0 ^ { \circ }} \mathbf{C}$ to $+\mathbf{8 5}{ }^{\circ} \mathbf{C}$, unless otherwise noted. Specifications to $-40^{\circ} \mathrm{C}$ are guaranteed by design, not production tested.)

| PARAMETER | CONDITIONS | MIN | TYP MAX | UNITS |
| :---: | :---: | :---: | :---: | :---: |
| MAIN/AFE STEP-UP DC-DC CONVERTER (MAX8610/MAX8612) |  |  |  |  |
| Step-Up Voltage Adjust Range |  | 2.5 | SU | V |
| FB_Regulation Voltage | No load | 0.995 | 1.025 | V |
| n-Channel On-Resistance |  |  | 0.175 | $\Omega$ |
| p-Channel On-Resistance |  |  | 0.25 | $\Omega$ |
| n-Channel Current Limit |  | 2.25 | 2.75 | A |
| MAIN/AFE STEP-DOWN DC-DC CONVERTER (MAX8611/MAX8613/MAX8611V) |  |  |  |  |
| Step-Down Voltage Adjust Range |  | 1 | SU | V |
| FB_Regulation Voltage | No load | 0.995 | 1.025 | V |
| n-Channel On-Resistance |  |  | 0.175 | $\Omega$ |
| p-Channel On-Resistance |  |  | 0.25 | $\Omega$ |
| p-Channel Current Limit |  | 0.9 | 1.1 | A |
| SD STEP-DOWN DC-DC CONVERTER |  |  |  |  |
| SD Step-Down Voltage Adjust Range |  | 1 | SU | V |
| FBSD Regulation Voltage | No load | 0.995 | 1.025 | V |
| n-Channel On-Resistance |  |  | 0.175 | $\Omega$ |
| p-Channel On-Resistance |  |  | 0.25 | $\Omega$ |
| p-Channel Current Limit |  | 0.9 | 1.1 | A |
| CCD BST DC-DC CONVERTER |  |  |  |  |
| BST Voltage Adjust Range |  | BATT | 27 | V |
| FBBST Regulation Voltage | No load | 0.995 | 1.025 | V |
| Load Switch On-Resistance |  |  | 0.15 | $\Omega$ |
| SWBST Current Limit |  | 0.7 | 0.9 | A |
| SWBST Short-Circuit Current Limit |  | 0.95 | 1.15 | A |
| CCD INV DC-DC CONVERTER |  |  |  |  |
| INV Voltage Adjust Range |  | $\begin{gathered} \text { PVINV } \\ -16 \end{gathered}$ | 0 | V |
| FBINV Regulation Voltage | No load | +10 | -10 | mV |
| HVPMOS On-Resistance |  |  | 1.0 | $\Omega$ |
| HVPMOS Current Limit |  | 0.65 | 0.85 | A |

## 8-Channel PMICs for Digital Camera Power Supplies

## ELECTRICAL CHARACTERISTICS (continued)

(BATT $=$ PVINV $=$ PVLED $=$ PVBST $=P V S D=P V M=P V A F E=3.6 V, P V S U=S U=5 V$, GND $=P G S U=P G M=P G A F E=P G S D=$ PG1 $=$ PG2 $=0 \mathrm{~V}, \mathrm{C}_{\text {REF }}=0.22 \mu \mathrm{~F}$, RREXT $=100 \mathrm{k} \Omega$ to $\mathrm{GND}, \mathrm{T}_{\mathbf{A}}=\mathbf{- 4 0 ^ { \circ }} \mathbf{C}$ to $\mathbf{+ 8 5} \mathbf{\circ} \mathbf{C}$, unless otherwise noted. Specifications to $-40^{\circ} \mathrm{C}$ are guaranteed by design, not production tested.)

| PARAMETER | CONDITIONS | MIN | TYP MAX | UNITS |
| :---: | :---: | :---: | :---: | :---: |
| LED BST DC-DC CONVERTER |  |  |  |  |
| LED Voltage Adjust Range |  | BATT | 27 | V |
| FBHLED Regulation Voltage | No load, FBLED $=0 \mathrm{~V}$ | 1.00 | 1.03 | V |
| FBLLED Regulation Voltage | No load, FBHLED $=0 \mathrm{~V}$ | 215 | 255 | mV |
| Load Switch On-Resistance |  |  | 0.15 | $\Omega$ |
| SWLED Current Limit |  | 0.7 | 0.9 | A |
| SWLED Short-Circuit Current Limit |  | 0.95 | 1.15 | A |
| AUXILIARY CONTROLLER |  |  |  |  |
| FBAUX Regulation Voltage (MAX8610/MAX8611/MAX8611V) |  | 1.23 | 1.26 | V |
| FBAUX Regulation Voltage (MAX8612/MAX8613) |  | -10 | +10 | mV |
| CCAUX Maximum Output Current | Sourcing or sinking | 90 |  | $\mu \mathrm{A}$ |
| DRVAUX On-Resistance | Output high or low |  | 10 | $\Omega$ |
| LOGIC INPUTS |  |  |  |  |
| ONSU Input Low Level | $1.5 \mathrm{~V}<\mathrm{PVSU}=\mathrm{SU}=\mathrm{BATT}<5.5 \mathrm{~V}$ |  | 0.5 | V |
| ONSU Input High Level | $1.5 \mathrm{~V}<\mathrm{PVSU}=\mathrm{SU}=\mathrm{BATT}<5.5 \mathrm{~V}, \mathrm{VH}$ is higher of PVSU and BATT | VH-0.2V with a max of 1.6 V |  | V |
| ONM, ONAFE, ONSD, ONBST, ONINV, ONLED, ONAUX Input Low Level | $3.3 \mathrm{~V}<\mathrm{PVSU}=\mathrm{SU}=$ BATT $<5.5 \mathrm{~V}$ |  | 0.5 | V |
| ONM, ONAFE, ONSD, ONBST, ONINV, ONLED, ONAUX Input High Level | $3.3 \mathrm{~V}<\mathrm{PVSU}=\mathrm{SU}=\mathrm{BATT}<5.5 \mathrm{~V}$ | 1.6 |  | V |
| SEQCCD Input Low Level | 3.3 V < PVSU $=$ SU $=$ BATT $<5.5 \mathrm{~V}$ |  | 0.5 | V |
| SEQCCD Input High Level | $\mathrm{PVSU}=\mathrm{SU}=\mathrm{BATT}=3.3 \mathrm{~V}$ | 2.3 |  | V |
|  | $\mathrm{PVSU}=\mathrm{SU}=\mathrm{BATT}=5.5 \mathrm{~V}$ | 3.4 |  |  |

Note 1: Once the step-up has reached regulation, the battery can decay to 0.9 V without loss of regulation.
Note 2: The idle-mode current threshold is the transition point between fixed-frequency PWM operation and idle-mode operation. The specification is given in terms of output load current for an inductor value of $2 \mu \mathrm{H}$. For the step-up, the idle-mode transition varies with input to the output-voltage ratio.
Note 3: Inverter line regulation is mostly a function of the converter duty factor, D, and is typically $20 \mathrm{mV}(\mathrm{D}-0.5)$.

# 8-Channel PMICs for Digital Camera Power Supplies 

## Typical Operating Characteristics

$\left(V_{\text {BATT }}=V_{\text {PVINV }}=V_{\text {PVLED }}=V_{\text {PVBST }}=V_{\text {PVSD }}=V_{\text {PVM }}=V_{\text {PVAFE }}=3.6 \mathrm{~V}, V_{\text {PVSU }}=V_{S U}=5 \mathrm{~V}\right.$, GND $=P G S U=P G M=P G A F E=P G S D$ $=$ PG1 $=$ PG2, CREF $=0.22 \mu F$, RREXT $=100 \mathrm{k} \Omega$ to GND. $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ (Circuit of Figure 2), unless otherwise noted.)


## 8-Channel PMICs for Digital Camera Power Supplies

Typical Operating Characteristics (continued)
$\left(V_{\text {BATT }}=V_{\text {PVINV }}=V_{\text {PVLED }}=V_{\text {PVBST }}=V_{\text {PVSD }}=V_{\text {PVM }}=V_{\text {PVAFE }}=3.6 \mathrm{~V}, V_{\text {PVSU }}=V_{S U}=5 \mathrm{~V}\right.$, GND $=P G S U=P G M=P G A F E=P G S D$ $=P G 1=P G 2, C_{\text {REF }}=0.22 \mu F$, RREXT $=100 \mathrm{k} \Omega$ to GND. $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ (Circuit of Figure 2), unless otherwise noted.)


## 8-Channel PMICs for Digital Camera Power Supplies

Typical Operating Characteristics (continued)
$\left(V_{\text {BATT }}=V_{\text {PVINV }}=V_{\text {PVLED }}=V_{\text {PVBST }}=V_{\text {PVSD }}=V_{\text {PVM }}=V_{\text {PVAFE }}=3.6 \mathrm{~V}, V_{\text {PVSU }}=V_{S U}=5 \mathrm{~V}\right.$, GND $=P G S U=P G M=P G A F E=P G S D$ $=$ PG1 = PG2, CREF $=0.22 \mu F$, RREXT $=100 \mathrm{k} \Omega$ to GND. $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ (Circuit of Figure 2), unless otherwise noted.)


MAX8610
MAIN AND STEP-DOWN
STARTUP WAVEFORMS


## 8-Channel PMICs for Digital Camera Power Supplies

$\left(V_{\text {BATT }}=V_{\text {PVINV }}=V_{\text {PVLED }}=V_{\text {PVBST }}=V_{P V S D}=V_{\text {PVM }}=V_{\text {PVAFE }}=3.6 \mathrm{~V}, V_{P V S U}=V_{S U}=5 \mathrm{~V}\right.$, GND $=P G S U=P G M=P G A F E=P G S D$ $=P G 1=P G 2, C_{\text {REF }}=0.22 \mu F$, RREXT $=100 \mathrm{k} \Omega$ to GND. $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ (Circuit of Figure 2), unless otherwise noted.)


MAX8610
AFE AS STEP-UP LOAD TRANSIENT
MAIN AS STEP-DOWN LOAD TRANSIENT


## 8-Channel PMICs for Digital Camera Power Supplies

Typical Operating Characteristics (continued)
$\left(V_{\text {BATT }}=V_{\text {PVINV }}=V_{\text {PVLED }}=V_{\text {PVBST }}=V_{\text {PVSD }}=V_{\text {PVM }}=V_{\text {PVAFE }}=3.6 \mathrm{~V}, V_{\text {PVSU }}=V_{S U}=5 \mathrm{~V}\right.$, GND $=P G S U=P G M=P G A F E=P G S D$ $=$ PG1 = PG2, CREF $=0.22 \mu F$, RREXT $=100 \mathrm{k} \Omega$ to GND. $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ (Circuit of Figure 2), unless otherwise noted.)

STEP-UP
LINE-TRANSIENT RESPONSE


STEP-DOWN
LINE-TRANSIENT RESPONSE


CCD
LINE-TRANSIENT RESPONSE


STEP-UP
LINE-TRANSIENT RESPONSE


STEP-DOWN LINE-TRANSIENT RESPONSE


SEQCCD HIGH THRESHOLD vs. STEP-UP VOLTAGE


## 8-Channel PMICs for Digital Camera Power Supplies

## Typical Operating Characteristics (continued)

$\left(V_{\text {BATT }}=V_{\text {PVINV }}=V_{\text {PVLED }}=V_{\text {PVBST }}=V_{P V S D}=V_{\text {PVM }}=V_{\text {PVAFE }}=3.6 \mathrm{~V}, V_{\text {PVSU }}=V_{S U}=5 \mathrm{~V}\right.$, GND $=P G S U=P G M=P G A F E=P G S D$ $=$ PG1 = PG2, CREF $=0.22 \mu F$, RREXT $=100 \mathrm{k} \Omega$ to GND. $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ (Circuit of Figure 2), unless otherwise noted.)

MAX8611V
STEP-UP (Vsu) SWITCHING WAVEFORMS

$4 \mu s / d i v$

MAX8611V
STEP-UP (VSU) SWITCHING WAVEFORMS


MAX8611V
STEP-DOWN (VAFE) SWITCHING WAVEFORMS

$2 \mu \mathrm{~s} / \mathrm{div}$

MAX8611
STEP-UP (VSu) SWITCHING WAVEFORMS

$2 \mu \mathrm{~s} / \mathrm{div}$

MAX8611
STEP-UP (VSU) DUAL SKIP SWITCHING WAVEFORMS


400ns/div

MAX8611
STEP-DOWN (Vafe) SWITCHING WAVEFORMS


# 8-Channel PMICs for Digital Camera Power Supplies 

Pin Description

| PIN | NAME | FUNCTION |  |
| :---: | :---: | :---: | :---: |
| 1 | ONINV | On/Off Control for the CCD Inverting Converter. Logic-high = on. The turn-on sequencing is governed by the SEQCCD pin; however, turn-on is locked out until the SU step-up DC-DC converter output has reached its final value. |  |
| 2 | FBM | Main Converter Feedback Input. The feedback threshold is 1.01V. This pin is high impedance in shutdown. |  |
| 3 | ONM | Main Converter On/Off Control. Logic-high = on; however, turn-on is locked out until the SU step-up DC-DC converter output has reached its final value. |  |
| 4 | PVM | MAX8610/MAX8612: Main Configured as a Step-Up with PVM as the Power Output. PVM is pulled to ground in shutdown. |  |
|  |  | MAX8611/MAX8613/MAX8611V: Main Configured as a Step-Down with PVM as the Power Input |  |
| 5 | LXM | Main Converter Switching Node. LXM is high impedance in shutdown. |  |
| 6 | PGM | Main Power Ground. Connect all PG_ pins to GND with short, wide traces as close to the device as possible. |  |
| 7 | PGAFE | AFE Power Ground. Connect all PG_ pins to GND with short, wide traces as close to the device as possible. |  |
| 8 | LXAFE | AFE Converter Switching Node. LXAFE is high impedance in shutdown. |  |
| 9 | PVAFE | MAX8610/MAX8612: AFE Configured as a Step-Up with PVAFE as the Power Output. PVAFE is pulled to GND in shutdown. |  |
|  |  | MAX8611/MAX8613/MAX8611V: AFE Configured as a Step-Down with PVAFE as the Power Input |  |
| 10 | ONAFE | AFE Converter On/Off Control. Logic-high = on; however, turn-on is locked out until the SU step-up DC-DC converter output has reached its final value. |  |
| 11 | FBAFE | AFE Converter Feedback Input. The feedback threshold is 1.01 V . This pin is high impedance in shutdown. |  |
| 12 | FBSD | Step-Down Converter Feedback Input. The feedback threshold is 1.01V. This pin is high impedance in shutdown. |  |
| 13 | PVSD | Step-Down Converter Input. Bypass to GND with a 10رF ceramic capacitor. |  |
| 14 | ONAUX | Auxiliary Controller On/Off Control. Logic-high = on; however, turn-on is locked out until the SU step-up DCDC converter output has reached its final value. |  |
| 15 | ONSD | SD Step-Down Converter On/Off Control. Logic-high = on; however, turn-on is locked out until the SU step-up DC-DC converter output has reached its final value. |  |
| 16 | LXSD | Step-Down Converter Switching Node. LXSD is high impedance in shutdown. |  |
| 17 | PGSD | Step-Down Power Ground. Connect all PG_ pins to GND with short, wide traces as close to the device as possible. |  |
| 18 | PG1 | Power Ground for One CCD Inverting Converter and Auxiliary Controller. Connect all PG_ pins to GND with short, wide traces as close to the device as possible. |  |
| 19 | DRVAUX | AUX Controller Gate-Drive Output. DRVAUX drives between PVINV and PG1. | MAX8610/MAX8611/MAX8611V: DRVAUX drives an n-channel FET in a boost configuration. DRVAUX is driven to GND in shutdown. |
|  |  |  | MAX8612/MAX8613: DRVAUX drives a p-channel FET in an inverter configuration. DRVAUX is driven to PVINV in shutdown. |
| 20 | PVINV | CCD Inverting Converter Input. Bypass to GND with a $1 \mu \mathrm{~F}$ ceramic capacitor. |  |
| 21 | LXINV | CCD Inverting Converter Switching Node. LXINV is high impedance in shutdown. |  |
| 22 | ONBST | On/Off Control for the CCD Boosting Converter. Logic-high = on. The turn-on sequencing is governed by the SEQCCD pin; however, turn-on is locked out until the SU step-up DC-DC converter output has reached its final value. |  |

## 8-Channel PMICs for Digital Camera Power Supplies

| PIN | NAME | FUNCTION |
| :---: | :---: | :---: |
| 23 | FBAUX | MAX8610/MAX8611/MAX8611V: Auxiliary Boost Controller Feedback Input. The feedback threshold is 1.25 V . This pin is high impedance in shutdown in the MAX8610/MAX8611V. This pin is shorted to GND in shutdown for MAX8611.. |
|  |  | MAX8612/MAX8613: Auxiliary Inverter Controller Feedback Input. The feedback threshold is OV. This pin is shorted to GND in shutdown. |
| 24 | CCAUX | Auxiliary Controller Compensation Node. This pin is pulled to GND in shutdown. |
| 25 | FBINV | CCD Inverting Converter Feedback Input. The feedback threshold is OV. This pin is shorted to GND in shutdown. |
| 26 | FBBST | CCD BST Converter Feedback Input. The feedback threshold is 1.01 V . This pin is high impedance in shutdown. |
| 27 | SEQCCD | When SEQCCD is low, the inverter and the boost start simultaneously if ONBST and ONINV are connected together. If not connected together, ONBST and ONINV have independent control. <br> When SEQCCD is high, the inverter is held off until the boost completes soft-start and is in regulation, and then begins its own soft-start. |
| 28 | GD | Gate-Drive Input for Internal MOSFET on the CCD BST and LED BST. Connect to BATT for Li+ and connect to PVSU for 2 AA. This pin is high impedance in shutdown. |
| 29 | PVBST | CCD BST Converter Input. Bypass to GND with a $1 \mu \mathrm{~F}$ ceramic capacitor. |
| 30 | SWBST | CCD BST True Shutdown Switch. The CCD BST inductor is connected between SWBST and LXBST. This pin is high impedance in shutdown. |
| 31 | LXBST | CCD BST Open-Drain Switching Inductor Node. The CCD BST inductor is connected between SWBST and LXBST. This pin is high impedance in shutdown. |
| 32 | PG2 | Power Ground to the CCDBST and LEDBST Converters. Connect all PG_ pins to GND with short, wide traces as close to the device as possible. |
| 33 | LXLED | LED Open-Drain Switching Inductor Node. The LED inductor is connected between SWLED and LXLED. This pin is high impedance in shutdown. |
| 34 | SWLED | LED True Shutdown Switch. The LED BST inductor is connected between SWLED and LXLED. This pin is high impedance in shutdown. |
| 35 | PVLED | LED BST Converter Power Input. Bypass to GND with a $1 \mu \mathrm{~F}$ ceramic capacitor. |
| 36 | ONLED | LED Converter On/Off Control. Logic-high = on; however, turn-on is locked out until the SU step-up DC-DC converter output has reached its final value. |
| 37 | FBLLED | The LED Boost Has Two Feedback Inputs, One for Current (FBLLED) and One for Maximum Voltage (FBHLED). The FBLLED feedback threshold is 0.24 V . The FBHLED threshold is 1.01 V . Soft-start is |
| 38 | FBHLED | provide a feedback path for soft-start. FBLLED and FBHLED are high impedance in shutdown. Connect FBLLED to GND if using only the FBHLED feedback. |
| 39 | REXT | Connect a $100 \mathrm{k} \Omega$ resistor from REXT to GND to program the internal OSC to 2 MHz . Connect a $200 \mathrm{k} \Omega$ resistor from REXT to GND to program the internal OSC to 1 MHz . See the Setting the Switching Frequency section. |
| 40 | REF | 1.25 V Reference Output. Bypass REF to GND with a $0.22 \mu \mathrm{~F}$ ceramic capacitor. This pin is internally pulled to GND in shutdown. |
| 41 | GND | Analog Ground. Connect to all PG_ pins as close to the device as possible. |
| 42 | FBSU | Step-Up Converter Feedback Input. The feedback threshold is 1.01V. This pin is high impedance in shutdown. |
| 43 | SU | Device Input Power Bootstrapped from PVSU. Connect PVSU and SU together. |
| 44 | PVSU | Step-Up Converter Output |

# 8-Channel PMICs for Digital Camera Power Supplies 

Pin Description (continued)

| PIN | NAME | FUNCTION |
| :---: | :---: | :--- |
| 45 | BATT | Power-Supply Input. Bypass with a 47 $\mu$ F ceramic capacitor. |
| 46 | ONSU | Step-Up Converter On/Off Control. Logic-high = on. All other ON_ pins are locked out until the SU step-up <br> DC-DC converter output has reached its final value. ONSU must be pulled high or toggled low then high after <br> BATT is present for the SU to start up. |
| 47 | LXSU | SU Step-Up Converter Switching Node. LXSU is high impedance in shutdown. |
| 48 | PGSU | SU Step-Up Power Ground. Connect all PG_ pins to GND with short, wide traces as close to the device as <br> possible. |
| - | EP | Exposed Metal Pad. This pad is internally connected to ground through a soft connect, meaning there is no <br> internal metal or bond wire physically connecting the exposed pad to the GND pin. Connecting the exposed <br> pad to ground does not remove the requirement for a good ground connection to the appropriate pins. For <br> good thermal dissipation, the exposed pad must be connected to the power ground plane. |

## Detailed Description

The MAX8610-MAX8613/MAX8611V can accept inputs from a variety of sources including 1 -cell $\mathrm{Li}+$ batteries, 2-cell alkaline or NiMH batteries, and systems designed to accept both battery types. All devices include seven DC-DC converter channels and one controller channel to build a multiple-output DSC powersupply system:

- Step-up DC-DC synchronous-rectified converter (_SU pins) with on-chip power FETs and True Shutdown.
- Main DC-DC synchronous-rectified converter (_M pins) with on-chip power FETs configured as a True Shutdown step-up (MAX8610/MAX8612) or stepdown (MAX8611/MAX8613/MAX8611V) DC-DC converter.
- Analog front-end (AFE) DC-DC synchronous-rectified converter (_AFE pins) with on-chip power FETs configured as a True Shutdown step-up (MAX8610/ MAX8612) or step-down (MAX8611/MAX8613/ MAX8611V) DC-DC converter.
- Core step-down DC-DC synchronous-rectified converter (_SD pins) with on-chip power FETs.
- CCD step-up DC-DC converter (_BST pins) with onchip power FET and an internal switch for True Shutdown.
- CCD inverting DC-DC converter (_INV pins) with on-chip power FET.
- WLED step-up DC-DC converter (_LED pins) with on-chip power FET and an internal switch for True Shutdown; includes constant current drive for white LEDs and open LED overvoltage protection. Can also be used for conventional boost applications.
- AUX DC-DC controller driving an external n-MOSFET for boost converters (MAX8610/MAX8611/ MAX8611V) or driving an external p-MOSFET for inverters (MAX8612/MAX8613).
A typical application circuit for the MAX8610 using 2 AA cell batteries is shown in Figure 1. Figure 2 shows a typical application circuit for a single-cell Li+ battery input using the MAX8611. Figure 2 can also operate in systems designed to be powered from both $\mathrm{Li}+$ and 2 AA cells.
All converters operate in a low-noise PWM mode with constant frequency and modulated pulse width under moderate to heavy loading. Efficiency is enhanced at light loads by switching to an idle mode where the converter switches only as needed to service the load. The synchronous-rectified converters (SU, MAIN, AFE, and SD) switch at a frequency set by an external resistor REXT (see the Setting the Switching Frequency section). The CCD and LED converters switch at one-half the frequency of the synchronous-rectified converters. The AUX controller switches at one-quarter the set switching frequency. Table 2 (see the Oscillator section) gives the switching frequency for each channel for oscillator frequencies of 1 MHz and 2 MHz .
Individual ON_ pins are provided for independent on/off control. The MAX8610-MAX8613/MAX8611V guarantee startup with an input voltage as low as 1.5 V and remain operational with input voltages down to 0.9 V . The MAX8610-MAX8613/MAX8611V also include overload protection and soft-start circuitry. See Figure 3 for the functional diagram.

8-Channel PMICs for Digital Camera Power Supplies
MAX8610-MAX8613/MAX8611V


Figure 1. MAX8610 (2 AA Input) Typical Application Circuit. The MAIN and AFE outputs operate as step-up converters.

# 8-Channel PMICs for Digital Camera Power Supplies 


^トト98XVW/E $198 X \forall W-0 / 98 X \forall W$

Figure 2. MAX8611 (Li+ or Combination Li+/2 AA Input) Typical Application Circuit. The MAIN (M) and AFE outputs operate as stepdown converters and are powered from the step-up (SU) for efficient boost-buck operation.

## 8-Channel PMICs for Digital Camera Power Supplies

MAX8610-MAX8613/MAX8611V


Figure 3. MAX8611 Functional Diagram

# 8-Channel PMICs for Digital Camera Power Supplies 


#### Abstract

The seven converter channels all use peak current-mode control and are internally compensated. These converters utilize a load line architecture to allow the output capacitor to be the dominant pole by lowering the loop gain. As a result, the MAX8610-MAX8613/MAX8611V match the load and line regulation to the voltage droop seen during transients. This is sometimes called voltage positioning. This architecture minimizes the voltage overshoot when the load is removed, and voltage droop during transition from a light load to full load (see the Load Transient graphs in the Typical Operating Characteristics). Thus, the voltage delivered to the load remains within spec more effectively than with regulators that might have tighter initial DC accuracy. This type of response is of great importance in digital cameras where the load may vary significantly in small time durations. See more details in the Load-Transient Response section. The AUX controller employs voltagemode control and needs external compensation (see the $A U X$ Compensation section).


## SU Step-Up DC-DC Converter

The SU step-up DC-DC switching converter typically generates a 5 V output voltage from a 1.5 V to 4.2 V battery input voltage, but any voltage from 3.3 V to 5 V can be set. The SU output voltage must be greater than or equal to the voltage output of the MAIN, AFE, and SD converters. An internal nFET switch and internal synchronous rectifier allow conversion efficiencies as high as $95 \%$. Under moderate to heavy loading, the converter operates in a low-noise PWM mode with constant frequency and modulated pulse width. Switching harmonics generated by fixed-frequency operation are consistent and easily filtered.
The SU step-up is a current-mode converter. The difference between the feedback voltage and a 1 V reference signal generates an error signal that programs the peak inductor current to regulate the output voltage. The peak inductor current limit is typically 2.5A. Inductor current is sensed across the internal switch and summed with an internal slope-compensation signal.
At light loads (less than 50mA (MAX8610-MAX8613)/ 125 mA (MAX8611V) when boosting to 5 V from a 3.6 V input), efficiency is enhanced by an idle mode in which switching occurs only as needed to service the load. This idle-mode threshold is determined by comparing the current-sense signal to an internal reference (Figure 3). In idle mode, the synchronous rectifier shuts off once its current falls to 10 mA , preventing negative inductor current.
In idle mode, the peak inductor current is fixed and the repetition rate is varied as required to keep the output voltage within the specified limits. In the MAX8610-

MAX8613, there are two skip levels for this peak inductor current in idle mode. For loads less than 50 mA (at $\mathrm{V}_{\mathrm{IN}}=$ 3.6 V and $\mathrm{VSU}=5 \mathrm{~V}$ ), a larger skip pulse $(400 \mathrm{~mA})$ is used to increase the time between pulses and enhance efficiency (see the MAX8611 Step-Up (VsU) Dual Skip Switching Waveforms in the Typical Operating Characteristics). For loads greater than 100 mA , a smaller skip pulse (200mA) is used to ensure that a pulse is given for every clock cycle (constant frequency operation) (see the MAX8611 Step-Up (VsU) Dual Skip Switching Waveforms in the Typical Operating Characteristics). In the MAX8611V, only a single skip level $(300 \mathrm{~mA})$ is used when the converter is in the idlemode operation (see the MAX8611V Step-Up (VSU) Switching Waveforms in the Typical Operating Characteristics). A single skip level results in higher efficiency for loads between 100 mA and 125 mA .
The step-up output, PVSU, can start up into a load (see the Typical Operating Characteristics). The soft-start duration is proportional to the size of the output cap and load resistor with a maximum of 7.5 ms . Under normal operation PVSU provides power to the device. After PVSU reaches regulation, the input voltage can drop as low as 0.9 V without affecting circuit operation (although available output power from the boost is reduced at very low inputs). All other outputs are locked out until the SU stepup reaches its regulation voltage. The step-up features True Shutdown, which eliminates the "sneak" body-diode path from input to output and allows the boost output to fall to GND in shutdown.

## MAIN and AFE Step-Up DC-DC Converter <br> (M and AFE, MAX8610/MAX8612)

 MAIN and AFE are configured as step-up converters in the MAX8610 and MAX8612. MAIN and AFE typically generate 3.3 V for system I/O and 3.4 V for the CCD analog front end, respectively. However, any voltage from BATT to VSU can be set.An internal nFET switch and internal synchronous rectifier allow conversion efficiencies as high as 93\%. Under moderate to heavy loading, the converter operates in a low-noise PWM mode with constant frequency and modulated pulse width. Switching harmonics generated by fixed-frequency operation are consistent and easily filtered.
At light loads (less than 50 mA when boosting to 5 V from a 1.8 V input), efficiency is enhanced by an idle mode in which switching occurs only as needed to service the load. The idle-mode current threshold is determined by comparing the current-sense signal to an internal reference (Figure 3). In idle mode, the synchronous rectifier shuts off once its current falls to 10 mA , preventing negative inductor current.

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The MAIN and AFE converters have True Shutdown. The output of the MAIN and AFE converters are pulled to GND in shutdown.

## MAIN and AFE Step-Down DC-DC Converter

 (M and AFE, MAX8611/MAX8613/MAX8611V) MAIN and AFE are configured as step-downs in the MAX8611/MAX8613/MAX8611V. MAIN and AFE derive power from PVM and PVAFE, respectively. These pins can be connected directly to BATT as long as the output is less than the battery voltage, or can be connected to the step-up output for efficient boost-buck operation. MAIN and AFE typically generate 3.3 V for the system I/O and 3.4 V for CCD sensor, respectively. However, any voltage from 1 V to 5 V that is less than or equal to the output of the step-up converter VSU can be set.An internal-MOSFET switch and synchronous rectifier allow conversion efficiencies as high as 90\% (boost-buck operation). Under moderate to heavy loading, the converter operates in a low-noise PWM mode with constant frequency and modulated pulse width. Switching harmonics generated by fixed-frequency operation are consistent and easily filtered. At light loads (typically less than 50mA (MAX8611/MAX8613)/125mA (MAX8611V)), efficiency is enhanced by an idle mode in which switching occurs only as needed to service the load.
In idle mode, the peak inductor current is fixed and the repetition rate is varied as required to keep the output voltage within the specified limits. In the MAX8610MAX8613, there are two skip levels for this peak inductor current in idle mode. For loads less than 50 mA (at $\mathrm{V}_{\mathrm{IN}}=$ 3.6 V and $\mathrm{V}_{S U}=5 \mathrm{~V}$ ), a larger skip pulse ( 400 mA ) is used to increase the time between pulses and enhance efficiency (see the MAX8611 Step-Up (VSU) Dual Skip Switching Waveforms in the Typical Operating Characteristics). For loads greater than 100 mA , a smaller skip pulse ( 200 mA ) is used to ensure that a pulse is given for every clock cycle (constant-frequency operation) (see the MAX8611 Step-Up (VSU) Dual Skip Switching Waveforms in the Typical Operating Characteristics). In the MAX8611V, only a single skip level ( 300 mA ) is used when the converter is in the idlemode operation (see the MAX8611V Step-Up (Vsu) Switching Waveforms in the Typical Operating Characteristics). A single skip level results in higher efficiency for loads between 100 mA and 125 mA .

## Li+ to 3.3V Boost-Buck Operation

When generating 3.3 V or a similar voltage from a Li+ cell, boost-buck operation may be needed so that a regulated output can be maintained for input voltages above and below 3.3V. In that case, it may be best to use the MAIN and AFE converters as step-downs (with
the MAX8611/MAX8613/MAX8611V) and to connect the inputs, PVM and PVAFE, to the step-up output (PVSU in Figure 2). The compound efficiency with this connection is typically up to $90 \%$. This connection is also suitable for designs that must operate from both $1-\mathrm{cell} \mathrm{Li}+$ and 2 AA cells. Note that the step-up output supplies both the step-up load and the input current of the MAIN and AFE step-downs so the MAIN and AFE input current reduces the available step-up output current for other loads.

## 2 AA Operation

In designs that operate only from 2 AA cells, the MAIN and AFE DC-DC converters operate as step-ups in the MAX8610/MAX8612. This connection is shown in Figure 1.

Step-Down DC-DC Converter (SD)
The SD step-down DC-DC converter is optimized to generate low output voltages (down to 1 V ) at high efficiency, typically to power a DSP core. The SD stepdown is powered from PVSD. PVSD can be connected directly to the battery if there is sufficient headroom; otherwise, it can be powered from the output of another converter. The SD step-down can also operate from the SU step-up (or another boost in the MAX8610/ MAX8612) for boost-buck operation.
Under moderate to heavy loading, the SD converter operates in a low-noise PWM mode with constant frequency and modulated pulse width. Efficiency is enhanced under light ( 50 mA typ) loading by assuming an idle mode during which the step-down switches only as needed to service the load.
In idle mode, the peak inductor current is fixed and the repetition rate is varied as required to keep the output voltage within the specified limits. In the MAX8610MAX8613 there are two skip levels for this peak inductor current in idle mode. For loads less than 50 mA (at V IN $=$ 3.6 V and V SU $=5 \mathrm{~V}$ ), a larger skip pulse ( 400 mA ) is used to increase the time between pulses and to enhance efficiency. For loads greater than 100 mA , a smaller skip pulse ( 200 mA ) is used to ensure that a pulse is given for every clock cycle (constant frequency operation). In the MAX8611V, only a single skip level ( 300 mA ) is used when the converter is in the idle-mode operation. A single skip level results in higher efficiency for loads between 100 mA and 125 mA .
The soft-start time for SD is shorter relative to M and AFE in order to maintain tracking during power-up. SD typically has a lower output voltage, so if SD is set to 1.2 V and M or AFE (MAX8611/MAX8613/MAX8611V) is set to 3.3 V , the two outputs track up to the point where both reach 1.2 V , if the two converters are enabled at the same time. The SD step-down DC-DC converter is inactive until the SU step-up DC-DC converter is in regulation.

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Table 1. Truth Table for SEQCCD, ONBST, and ONINV

| ONINV | ONBST | SEQCCD | BST O/P | INV O/P |
| :---: | :---: | :---: | :---: | :---: |
| $H$ | H | L | On | On |
| H | L | L | Off | On |
| L | H | L | On | Off |
| L | L | L | Off | Off |
| X | L | H | Off | Off |
| L | H | H | On | Off |
| $H$ | H | On | On (turns on after BST <br> is in regulation) |  |

## LED and CCD, BST, and INV Converters

The MAX8610-MAX8613/MAX8611V include a boost and inverting DC-DC converter to supply both positive and negative CCD (and/or LCD) bias and WLED supply. All converters use a fixed-frequency, PWM currentmode control scheme. The heart of the current-mode PWM controllers is a comparator that compares the feedback error signal against the sum of the amplified current-sense signal and a slope-compensation ramp. At the beginning of each clock cycle, the internal power switch turns on until the PWM comparator trips. During this time the current in the inductor ramps up, storing energy in the inductor's magnetic field. When the power switch turns off, the inductor releases the stored energy while the current ramps down, providing current to the output. These converters operate at one-half the frequency of the SU, M, AFE, and SD converters.

## LED and CCD Boost Converter (BST)

The CCD boost converter generates a positive output voltage up to 27 V . An internal power switch, internal True Shutdown switch, and external catch diode allow conversion efficiencies as high as $90 \%$.
The internal True Shutdown switch disconnects the battery from the load by opening the battery connection to the inductor. The True Shutdown switch stays on at all times during normal operation. The boost converter also features soft-start to limit inrush current and minimize battery loading at startup. This is accomplished by ramping the reference voltage at the input of the error amplifier. The boost reference is ramped from 0 to 1V (where 1V is the desired feedback voltage). During startup, the boost-converter load switch turns on before the boost-converter reference voltage is ramped up. This effectively limits startup inrush current to below 500 mA and provides short-circuit protection (SCP).

## CCD Inverter (INV)

The inverter generates output voltages down to -10V. An internal power switch and external catch diode allow conversion efficiencies as high as $90 \%$. The inverter soft-starts by ramping the reference input of the error amplifier from 1.25 V to OV (where OV is the inverter's normal operating feedback point).

## Power-On Sequencing (SEQ)

The CCD boost and inverter have pin-selectable power-on sequencing as set by the SEQCCD pin (see Table 1 and the Typical Operating Characteristics). This covers all typical sequencing options required by CCD imagers. The SEQCCD should be connected to Vsu for a high level and to GND for a low level. See the Typical Operating Characteristics for the SEQCCD threshold as a function of the SU converter output voltage VSU.
When SEQCCD $=0$ and both ONBST and ONINV are pulled high together, both outputs reach regulation at approximately the same time. The inverter is held off while the boost load switch slowly turns ON to pull SWBST to VBATT. The positive output rises to a diode drop below $V_{\text {BATT }}$. Once the boost output reaches this voltage, the boost and the inverter then ramp their respective references over a period of 7.5 ms . This brings the two outputs into regulation at approximately the same time.
When SEQCCD $=1$ and both ONBST and ONINV are pulled high together, the boost output powers on first. The inverter is held off until the boost completes its entire soft-start cycle and the positive output is in regulation. Then the inverter starts its soft-start cycle and achieves regulation in approximately 7.5 ms .
When SEQCCD $=0$ if ONBST and ONINV are not connected together, then there is no internal power-up sequencing and the two converters can be independently controlled with the respective ON pins.

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Figure 4. AUX Boost-Controller Block Diagram

## AUX Controller

One auxiliary DC-DC controller is provided for an additional boost or inverter channel. On the MAX8610/ MAX8611/MAX8611V, the AUX controller drives an external n-channel MOSFET in a boost configuration. On the MAX8612/MAX8613, the AUX controller drives an external p-channel MOSFET in an inverter configuration. Since the controller does not include internal power MOSFETs, output power and efficiency is determined largely by external components.
The AUX controller regulates output voltage by modulating the pulse width of DRVAUX based on the feedback input at FBAUX. The controller is voltage mode and requires external compensation at CCAUX. AUX operates at $1 / 4$ the frequency of the SU, MAIN, AFE, and SD converters.
Figures 4 and 5 show functional diagrams of AUX boost and inverter controllers. A sawtooth oscillator signal at OSC governs timing. At the start of each cycle, during normal operation DRVAUX goes high on the MAX8610/ MAX8611/MAX8611V, turning on the external nFET switch (DRVAUX goes low on the MAX8612/MAX8613 to turn on a pFET switch for the inverter). The switch then turns off when the internally level-shifted sawtooth crosses CCAUX or when the maximum duty cycle is exceeded. The switch remains off until the start of the next cycle.

Maximum Duty Cycle
The AUX PWM controllers have a guaranteed maximum duty cycle of $86 \%$ and typically can reach $87.5 \%$. In designs that require continuous inductor current (where the inductor does not discharge to zero at the end of


Figure 5. AUX Inverter-Controller Block Diagram
each switching cycle), the maximum duty cycle limits the boost ratio so that:

$$
\text { DBST }=1-(\mathrm{V} \text { IN } / \text { VOUT })<86 \%
$$

or, for inverters, it limits the ratio so that:
DINV = IVOUTI / (IVOUTI +VIN) < 86\%

Note that with discontinuous inductor current, no such limit exists for the input/output ratio since the inductor has time to fully discharge before the next cycle begins.

## Soft-Start

All DC-DC converter channels feature soft-start to limit inrush current and prevent excessive battery loading at startup by ramping the output voltage of each channel up to the regulation voltage. This is accomplished by ramping the internal reference inputs to each channel error amplifier when a channel is enabled.
The soft-start ramps for most channels take 15,000 OSC cycles (or 15 ms for a 1 MHz oscillator). One exception is the SD step-down converter, where the soft-start ramp takes 5000 OSC cycles. The soft-start time for SD is less relative to other channels in order to match power-up tracking since SD typically has a lower output voltage. Note, however, that no channels start until the SU step-up reaches regulation.

## Fault Protection

The MAX8610-MAX8613/MAX8611V have robust fault and overload protection. After power-up, the device is set to detect an out-of-regulation state that could be caused by an overload or short. If any DC-DC converter channel remains faulted for 200,000 clock cycles

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Table 2．Switching Frequency for Each Converter Channel

| $\begin{gathered} \text { REXT } \\ (k \Omega) \end{gathered}$ | $\underset{\text { (MHz) }}{\mathrm{SU}}$ | $\begin{aligned} & \text { MAIN } \\ & \text { (MHz) } \end{aligned}$ | $\begin{gathered} \text { AFE } \\ \text { (MHz) } \end{gathered}$ | $\begin{gathered} \mathrm{SD} \\ (\mathrm{MHz}) \end{gathered}$ | $\begin{gathered} \hline \text { CCDBST } \\ \text { (MHz) } \end{gathered}$ | $\begin{aligned} & \text { CCDINV } \\ & \text { (MHz) } \end{aligned}$ | LEDBST <br> （MHz） | AUX <br> （MHz） |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 100 | 2 | 2 | 2 | 2 | 1 | 1 | 1 | 0.5 |
| 200 | 1 | 1 | 1 | 1 | 0.5 | 0.5 | 0.5 | 0.25 |

（200ms at 1 MHz OSC），then all outputs latch off until the step－up DC－DC converter is reinitialized by the ONSU pin．
Once the step－up output is in regulation，if the SU hits current limit for 200，000 consecutive clock cycles，the device enters a fault condition．If the step－up output （PVSU）is dragged 10\％below its regulation voltage or is shorted，the device enters a fault state immediately． The step－up then shuts down all channels．All outputs stay latched off until the step－up DC－DC converter is reinitialized by the ONSU pin．
If the short at SU exists prior to ONSU being pulled high， then the SU DC－DC converter continuously cycles through soft－start once ONSU is pulled high since VSU never goes above its 3 V UVLO threshold．The part continues to draw approximately 1A of input current in this condition．The user is recommended to monitor such a condition and pull ONSU low to prevent thermal runaway．
In systems where a submicroprocessor（sub－$\mu \mathrm{P}$ ）is used， the output of the MAIN converter is diode－ORed with the backup power supply to supply power to the sub－$\mu \mathrm{P}$ ． The sub－$\mu \mathrm{P}$ also controls the power－on signal going to ONSU to turn on the MAX8610－MAX8613／MAX8611V． Under these circumstances，the sub－$\mu \mathrm{P}$ can be used to monitor the 3．3V MAIN supply and pull ONSU low if a startup into a short－circuit prevents the 3．3V MAIN supply from turning on within a specified time（1s，for example）．
In the CCDBST and LEDBST converters an overload／ short condition stops converter switching immediately． The True Shutdown switch limits the inductor current to 1 A maximum for 200,000 clock cycles．If the overload／ short－circuit condition persists beyond this time，then the device enters a fault condition．All channels are shut down and stay latched off until the step－up DC－DC con－ verter is reinitialized by the ONSU pin．If the overload／ short－circuit condition is removed within the 200，000 clock cycles，soft－start is reinitiated．
For all other channels an overload／short－circuit condition for over 200，000 clock cycles on the output are detected as a fault．Once in fault，all channels are shut down and stay latched off until the step－up DC－DC converter is reinitialized by the ONSU pin．

Reference
The MAX8610－MAX8613／MAX8611V have a precise 1.250 V reference at REF．Bypass REF to GND with a $0.22 \mu \mathrm{~F}$ ceramic capacitor．REF can source up to $100 \mu \mathrm{~A}$ for external loads．REF is enabled whenever ONSU is high and PVSU is above 3 V ．During shutdown REF is internally pulled to GND．

Oscillator
The operating frequency is set by a resistor connected from REXT to GND．The range of usable settings is from 1 MHz to 2 MHz ．Note that although all converter channels are synchronized，they do not operate at the same frequency．The SU，MAIN，AFE，and SD converters all switch at the set oscillator frequency．The CCDBST and INV converters，as well as the LEDBST，switch at one－half the oscillator frequency，and the AUX controller switches at one－quarter the oscillator frequency．The CCDBST， INV，and AUX converters switch at reduced rates to opti－ mize efficiency for those channels．Table 2 details each converter＇s operating frequency for 1 MHz and 2 MHz oscillators．See also Setting the Switching Frequency in the Design Procedure section．

## Shutdown

The SU step－up converter is activated with a high input signal at ONSU．All other converters are individually acti－ vated with logic－high levels on their respective ON＿ inputs．For automatic startup of any channel，connect its ON＿pin to PVSU or a logic level greater than 1．6V． Connecting all ON＿to GND or logic 0 places the MAX8610－MAX8613／MAX8611V in shutdown mode and reduces supply current to $0.1 \mu \mathrm{~A}$ ．In shutdown，the control circuitry，internal switching MOSFETs，and synchronous rectifiers turn off and LX＿becomes high impedance．
All converter channels（except AUX）provide True Shutdown so that no current flows from the battery to the load during shutdown．Unlike conventional boost converters，no external switch circuitry is needed to block battery drain in shutdown．
SEQCCD does not have a logic－level threshold．SEQC－ CD should be connected to VSU for a high level and to GND for a low level．See the Typical Operating Characteristics for the SEQCCD threshold as a function of the SU converter output voltage $\mathrm{V}_{\text {SU }}$ ．

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## Design Procedure

## Setting the Switching Frequency

Choose a switching frequency to optimize external component size or circuit efficiency for the particular application. Typically, switching frequencies between 1 MHz and 2 MHz offer a good balance between component size and circuit efficiency-higher frequencies generally allow smaller components, while lower frequencies give better conversion efficiency. The switching frequency is set with an external timing resistor connected from REXT to GND. The REXT value for a particular oscillator frequency is:

$$
\text { REXT }(k \Omega)=(200) / f o s c(M H z)
$$

## Setting Output Voltages

All MAX8610-MAX8613/MAX8611V output voltages are resistor set. The FB_ threshold is 1 V for all channels except for FBLLED (0.24V), FBINV (0V), and FBAUX (1.25V) for the AUX boost on the MAX8610/MAX8611/ MAX8611V, and (0V) for the AUX inverter on the MAX8612/MAX8613. When setting the output voltage for any boost or step-down channel, connect a resistive volt-age-divider from the channel output to the corresponding FB_ input and then to GND. The FB_ input bias current is less than 50nA, so choose the bottom-side (RBOTtOM from FB_ to GND) resistor to be $100 \mathrm{k} \Omega$ or less. Then calculate the top-side (RTOP from output to FB_) resistor:

$$
\text { RTOP }=\text { RBOTtOM[(VOUT / VFB_) - 1] }
$$

where $V_{F B}$ is the feedback regulation voltage of the particular DC-DC converter channel (1V for FBSU, FBM, FBAFE, FBSD, FBBST, and FBHLED, or 1.25 V for the MAX8610/MAX8611/MAX8611V FBAUX).

## Setting Inverter Output Voltages

All devices feature a CCD inverter. The CCD inverter feedback input is at FBINV and has a threshold of OV. To set the negative output voltage, connect a resistive voltage-divider from the negative output (VCCDINV) to the FBINV input, and then to REF. The FBINV input bias current is less than 50nA, so choose the FBINV-to-REF resistor, RREF (R8 in Figures 1 and 2), to be $100 \mathrm{k} \Omega$ or less. Then calculate the output-to-FBINV resistor, RINV (R7 in Figures 1 and 2), as follows:
RINV = RREF(|VCCDINVI/ 1.25)

A second inverter is available by using the AUX controller on the MAX8612/MAX8613. The formula for calculating feedback resistors for the inverting AUX controller is the same as above.

## Setting LED Current and Voltage

When using the LED boost as a current source to drive white (or other) LEDs, connect an LED current-sense
resistor from FBLLED to GND. Select the LED currentsetting resistor (R17 in Figures 1 and 2) using the following formula:

$$
\mathrm{R} 17=0.24 \mathrm{~V} / \mathrm{ILED}
$$

where lLED is the regulated current in the series LED string. The LED boost also allows a voltage limit to be set with FBHLED so that if the LED string becomes open circuit, the output voltage is still regulated. The limit voltage should be selected to be 1 V higher than the maxi-mum-expected LED forward voltage (VMAXLED), but no higher than 27 V . Choose the bottom-side (R16 from FBHLED to GND in Figures 1 and 2) resistor to be $100 \mathrm{k} \Omega$ or less. Then calculate the top-side (R15 from VLED to FBHLED in Figures 1 and 2) resistor:

$$
\mathrm{R} 15=\mathrm{R} 16\left[\mathrm{~V}_{\text {MAXLED }}\right]
$$

Note that the VLED output VBOOST can instead be used as a high-voltage boost for any function, by using only R15 and R16 to set voltage and by omitting R17 and grounding FBLLED. In that case:

$$
\mathrm{R} 15=\mathrm{R} 16\left[\mathrm{~V}_{\text {BOOST }}-1\right]
$$

Filter Capacitor Selection
The input capacitor in a DC-DC converter reduces current peaks drawn from the battery or other input power source and reduces switching noise in the controller. The impedance of the input capacitor at the switching frequency should be less than that of the input source so high-frequency switching currents do not pass through the input source.
The DC-DC converter output filter capacitors keep output ripple small and ensure control-loop stability. The output capacitor must also have low impedance at the switching frequency. Ceramic, polymer, and low-ESR tantalum capacitors are suitable, with ceramic exhibiting the lowest ESR and high-frequency impedance. Output ripple with a ceramic output capacitor is approximately as follows:

$$
V_{\text {RIPPLE }}=\operatorname{l}(\text { PEAK })[1 /(2 \pi \text { fOSC COUT })]
$$

If the capacitor has significant ESR, the output ripple component due to capacitor ESR is as follows:

$$
\mathrm{V}_{\mathrm{RIPPLE}}(\mathrm{ESR})=\mathrm{I}_{\mathrm{L}(\mathrm{PEAK})} \mathrm{ESR}
$$

## Step-Up Component Selection

This section describes component selection for the SU step-up, as well as for the MAIN and AFE step-up that are found on the MAX8610 and MAX8612. The external components required for the step-up are an inductor and input and output filter capacitors. The inductor is typically selected to operate with continuous current for best efficiency. An exception might be if the step-up ratio, (VOUT / VIN), is greater than 1 / (1-DMAX), where

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DMAX is the maximum PWM duty factor stated in the Electrical Characteristics table.
In most step-up designs, a reasonable inductor value (LIDEAL) can be derived from the following equation, which sets continuous peak-to-peak inductor current at 1/3 the DC inductor current:

$$
\text { LIDEAL }=[3.5 \mathrm{~V} \text { IN(MIN) D (1-D)] / (IOUT fOSC) }
$$

where $D$ is the duty factor given by:

$$
\mathrm{D}=1-\left(\mathrm{V}_{\text {IN }} / \mathrm{V}_{\text {OUT }}\right)
$$

Given LIDEAL, the consistent peak-to-peak inductor current is IOUT / [3(1-D)]. The peak inductor current, $\operatorname{IL}($ PEAK $)=1.25$ IOUT / (1-D). Inductance values smaller than LIDEAL can be used to reduce inductor size; however, if much smaller values are used, inductor ripple current rises and a larger output capacitance may be required to suppress output ripple.

## Step-Down Component Selection

This section describes component selection for the SD step-down converter and for the MAIN and AFE stepdowns that are found on the MAX8611/MAX8613/ MAX8611V. The external components required for the step-down are an inductor and input and output filter capacitors. The step-down converters provide best efficiency with continuous inductor current. A reasonable inductor value (LIDEAL) can be derived from the following equation:

LIDEAL $=\left[3\left(\mathrm{~V}_{\text {IN }}\right) \times \operatorname{DSD}\left(1-\mathrm{DSD}^{2}\right)\right] /($ IOUT fOSC $)$

This sets the peak-to-peak inductor current at $1 / 3$ the DC inductor current. DSD is the step-down switch duty cycle: DSD = VOUT / VIN.
Given LIDEAL, the peak-to-peak inductor current is IOUT / 3. The absolute-peak inductor current is 1.25 IOUT. Inductance values smaller than LIDEAL can be used to reduce inductor size; however, if much smaller values are used, inductor ripple current for a given load rises, and a larger output capacitance may be required to suppress output ripple. Larger values than LIDEAL can be used to obtain higher output current, but typically with larger inductor size.

## LED and CCD Component Selection

CCD/LED Inductor Selection
The LED boost, CCD boost, and CCD inverter's high switching frequency (fosc / 2) allows for the use of small inductors. The $10 \mu \mathrm{H}$ inductors (L5, L6, and L7) shown in the typical operating circuits are recommended for most applications. Smaller inductances require less board space, but may cause greater peak current due to current-sense comparator propagation delay.
Use inductors with a ferrite core or equivalent. Powder iron cores are not recommended for use with high switching frequencies. The inductor's incremental saturation rating must meet or exceed the LXBST, LXINV, and LXLED current limits. For highest efficiency, use inductors with a low DC resistance (under $100 \mathrm{~m} \Omega$ ). Table 3 is the LED and CCD inductor selection guide.

Table 3. LED and CCD Inductor Selection Guide

| OUTPUT VOLTAGES AND LOAD CURRENT | INDUCTOR | $\mathrm{L}(\mu \mathrm{H})$ | DCR (m $)^{\text {) }}$ | ISAT (A) | SIZE (mm) |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\begin{gathered} 15 \mathrm{~V}, 50 \mathrm{~mA} ; \\ -7.5 \mathrm{~V}, 100 \mathrm{~mA} \end{gathered}$ | $\begin{array}{\|l\|} \hline \text { TOKO } \\ \text { DP418C } \\ \text { S1024AS-4R3M } \end{array}$ | 4.3 | 47 | 1.2 | $4 \times 4 \times 1.7$ |
|  | Sumida CDRH2D14-4R7 | 4.7 | 170 | 1 | $3.2 \times 3.2 \times 1.55$ |
|  | TOKO <br> DP418C <br> S1024AS-100M | 10 | 100 | 0.8 | $4 \times 4 \times 1.7$ |
| $\begin{aligned} & 15 \mathrm{~V}, 20 \mathrm{~mA} ; \\ & -7.5 \mathrm{~V}, 40 \mathrm{~mA} \end{aligned}$ | TOKO <br> DP418C <br> S1024AS-4R3M | 4.3 | 47 | 1.2 | $4 \times 4 \times 1.7$ |
|  | Sumida CDRH2D14-4R7 | 4.7 | 170 | 1 | $3.2 \times 3.2 \times 1.55$ |
|  | TOKO <br> DP3015C <br> S1068AS-4R7M | 4.7 | 155 | 0.9 | $3 \times 3 \times 1.5$ |

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## CCD/LED Diode Selection

High switching frequency (fosc / 2) demands a highspeed rectifier. Schottky diodes, such as the CMHSH5-2L or MBR0530L, are recommended. Make sure that the diode's peak current rating exceeds the selected current limit, and that its breakdown voltage exceeds the output voltage. Schottky diodes are preferred due to their low forward voltage. However, ultra-high-speed silicon rectifiers are also acceptable.

CCD/LED Output Filter Capacitors
For most applications, $10 \mu \mathrm{~F}$ ceramic output filter capacitors are suitable for the CCD outputs. Lower values may be acceptable to save space at low output currents or if higher ripple can be tolerated. The minimum capacitor values required for stability are calculated as follows:
For CCD and LED boost output stability, the filter capacitor, CBST, should satisfy:

$$
\text { CBST > }(10 \mathrm{~L} \text { IBST }) /\left(\operatorname{RCS}\left(1-\mathrm{DBST}^{\text {B }}\right) \mathrm{V}_{\mathrm{BST}}{ }^{2}\right)
$$

where IBST is the output current, V V $_{\text {BST }}$ is the output voltage, Rcs $=0.015$, and DBST is the boost switch duty cycle: DBST = 1 - (VBATT / VBST).
For CCD inverter stability, the filter capacitor, CINV, should satisfy the following:

$$
\mathrm{C}_{\text {INV }}>\frac{3 L V_{\text {REF }} I_{\text {INV }}}{R_{\mathrm{CS}}\left(1-D_{\text {INV }}\right)\left(V_{\text {REF }}-V_{\text {INV }}\right) V_{\text {INV }}}
$$

where IINV is the output current, VINV is the output voltage, Rcs $=0.015$, and Dinv is the inverter switch duty cycle: Dinv = IVINvI / (IVinvl +VPVINV).
Table 3 lists representative inductors for the LED and CCD outputs.

## AUX Controller Component Selection

 External MOSFETThe AUX controller drives an external logic-level MOSFET. Significant MOSFET selection parameters are as follows:

- On-resistance (RDS(ON))
- Maximum drain-to-source voltage (VDS(MAX))
- Total gate charge (QG)
- Reverse transfer capacitance (CRSS)

On the MAX8610/MAX8611/MAX8611V the AUX driver, DRVAUX, is designed for n-channel MOSFETs. On the MAX8612/MAX8613, AUX is a DC-DC inverting controller, so DRVAUX is designed to drive a p-channel MOSFET. In all devices, DRVAUX swings between PVINV and PG1. Use a MOSFET with on-resistance specified with a gate drive at or below the PVINV voltage.
The MOSFET gate charge, $Q_{G}$, includes all capacitance associated with charging the gate and helps to
predict MOSFET transition time between on and off states. MOSFET power dissipation is a combination of on-resistance and transition losses. The on-resistance loss is as follows:
PRDSON = D I L² RDS(ON)
where $D$ is the duty cycle, $I_{L}$ is the average inductor current, and $\operatorname{RDS}(O N)$ is MOSFET on-resistance. The transition loss is approximately as follows:

$$
\text { PTRANS }=(\text { Vout IL fosc tT) / } 3
$$

where VOUT is the output voltage, I L is the average inductor current, fosc is the switching frequency, and to is the transition time. The transition time is approximately $Q_{G} / I_{G}$, where $Q_{G}$ is the total gate charge, and IG is the gate-drive current ( 0.5 A typ). The total power dissipation in the MOSFET is as follows:
PMOSFET = PRDSON + PTRANS

## Diode

For most AUX applications, a Schottky diode rectifies the output voltage. The Schottky low forward voltage and fast recovery time provide the best performance in most applications. Silicon signal diodes (such as 1N4148) are sometimes adequate in low-current ( $<10 \mathrm{~mA}$ ), high-voltage ( $>10 \mathrm{~V}$ ) output circuits where the output voltage is large compared to the diode forward voltage.

## AUX Compensation

The auxiliary controller employs voltage-mode control to regulate the output voltage. Optimum compensation depends on whether the design uses continuous or discontinuous inductor current. Note that in the following discussions, $\mathrm{f}_{\mathrm{A}} \mathrm{X}$, the auxiliary controller switching frequency, is $1 / 4$ of the oscillator frequency set by REXT.

## MAX8610/MAX8611/MAX8611V AUX Step-Up, <br> Discontinuous Inductor Current

When the inductor current falls to zero on each switching cycle, it is described as discontinuous. The inductor is not utilized as efficiently as with continuous current, but in light-load applications this often has little negative impact since the coil losses may already be low compared to other losses. A benefit of discontinuous inductor current is more flexible loop compensation and no maximum duty-cycle restriction on boost ratio. To ensure discontinuous operation, the inductor must have a sufficiently low inductance to fully discharge on each cycle. This occurs when:

$$
\mathrm{L}<\left[\mathrm{VIN}^{2}\left(\mathrm{VOUT}^{-}-\mathrm{V} \operatorname{IN}\right) / \mathrm{VOUT}^{3}\right]\left[\text { RLOAD } /\left(2 \mathrm{f}_{\mathrm{AUX}}\right)\right]
$$

A discontinuous current boost has a single pole at the following frequency:

$$
\mathrm{fP}=\left(2 \mathrm{~V}_{\text {OUT }}-\mathrm{V}_{\text {IN }}\right) /(2 \pi \text { RLOAD COUT VOUT })
$$

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A type 2 compensation is recommended as shown in Figure 6.


Figure 6. Type 2 Compensation Circuit
The crossover frequency for the boost loop is given by: C1 $=[1 /(2 \pi \times f C \times R 1)]\left[V_{F B} / V_{\text {RAMP }}\right][R L O A D V o u t /$
(2Lfaux (VOUT - Vin)) $]^{1 / 2}[2 \mathrm{~V}$ IN / (2VOUT - VIN) $]$
where $V_{\text {RAMP }}$ is the internal slope-compensation voltage ramp of 1.25 V .
The frequency of the pole and zero are defined by the equations below. R2 and C1 introduce a zero at a frequency given by:

$$
\mathrm{fz}=1 /(2 \pi \mathrm{R} 2 \mathrm{C} 1)
$$

While a pole is introduced at the frequency:

$$
\mathrm{fP2} 2=1 /(2 \pi \mathrm{R} 2 \mathrm{C} 2)
$$

The following is a typical procedure for selecting the compensation components for a discontinuous-conduction mode boost.

- Choose the compensation so the unity-gain crossover, fc, occurs at fAUX / 10 or lower.
- Set the resistor-divider formed by R1 and RBIAS to set the desired output regulation voltage as specified in the Setting Output Voltages section. R1 = Rbias (Vout / 1.25-1) where Rbias is chosen to be $100 k \Omega$ or lower. Note that RBIAS only sets the DC operating point of the loop and has no effect on the AC characteristics.
- Set the zero fz formed by R2 and C1 at approximately the boost pole fp.
- Set the pole fP2 formed by R2 and C2 approximately equal to the ESR zero of the output capacitor or in case of ceramic capacitors, a decade below the crossover frequency fc.

MAX8610/MAX8611/MAX8611V AUX Step-Up, Continuous Inductor Current
Continuous inductor current can sometimes improve boost efficiency by lowering the ratio between peak inductor current and output current. It does this at the expense of a larger inductance value that requires larger size for a given current rating. With continuous-inductorcurrent boost operation, there is a right-half-plane zero, ZRHP, at:

$$
Z_{\text {RHP }}=(1-\mathrm{D})^{2} \text { RLOAD } /(2 \pi \mathrm{~L})
$$

where $D$ is the switch duty factor and $(1-\mathrm{D})=\mathrm{V} / \mathrm{N} /$ Vout (in a boost converter).
There is a complex pole pair at:

$$
\mathrm{fo}_{0}=\mathrm{V}_{\mathrm{IN}} /\left[2 \pi \text { VOUT }(\text { L COUT })^{1 / 2}\right]
$$

A type 3 error-amplifier compensation network can be used to optimize the loop response for the continuous conduction mode. The type 3 amplifier circuit is shown in Figure 7.


Figure 7. Type 3 Error-Amplifier Circuit
The frequency of the poles and zeros introduced by this compensation network are defined by the following equations.
The zeros are:

$$
\begin{gathered}
\mathrm{fZ} 1=1 /(2 \pi \mathrm{R} 2 \mathrm{C} 1) \\
\mathrm{fZ2}=1 /(2 \pi \mathrm{R} 1 \mathrm{C} 3) \text { (assuming R1>>R3) }
\end{gathered}
$$

The poles are:

$$
f P 1=1 /(2 \pi R 3 C 3)
$$

$$
\mathrm{fP2}=1 /(2 \pi \mathrm{R} 2 \mathrm{C} 2)(\text { assuming C1>>C2 })
$$

Also, the unity-gain frequency or crossover frequency is:

$$
f C=1 /(2 \pi R 1 C 1)
$$

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With voltage-mode control the goal of the loop design is to set the crossover frequency above the complex pole pair frequency but below the RHP zero. This is accomplished by placing the two zeros below the complex pole pair as this provides a phase boost. The two poles are then placed a decade above the crossover frequency. The following is a typical procedure for selecting the compensation components for a continu-ous-conduction-mode boost:

1) Choose the compensation so the unity-gain crossover, fc , occurs approximately a decade above the complex pole pair but at least before 1/6 the RHP zero frequency and $1 / 10$ the switching frequency faux.
2) Set the resistor-divider formed by R1 and RBIAS to set the desired output regulation voltage as specified in the Setting Output Voltages section:
R1 = RBIAS (VOUT / 1.25-1)
where $\mathrm{R}_{\mathrm{BIAS}}$ is chosen to be $100 \mathrm{k} \Omega$ or lower.
Note that RBIAS only sets the DC operating point of the loop and has no effect on the AC characteristics.
3) Compute C 1 knowing the crossover frequency fC and R1.
4) Set the zero fz2 formed by R1 and C3 approximately halfway between the complex pole pair and the crossover frequency $f \mathrm{c}$ to compensate for the phase loss.
5) Set the other zero fZ 1 formed by R2 and C1 approximately one-half decade above the complex pole pair.
6) If the zero due to the output capacitance and ESR (ZCOUT $=1 /(2 \pi$ COUT RESR)) is within a decade of the crossover frequency, then set the pole formed by R3 and C3 to cancel the ESR zero. If ZCOUT is much higher than $\mathrm{f}_{\mathrm{C}}$ (as is typical with ceramic output capacitors) and continuous conduction is required, then set the pole formed by R3 and C3 more than a decade higher than the crossover frequency.
7) Set the second pole formed by R2 and C2 (fp2) more than one-half a decade above the crossover frequency.

## MAX8612/MAX8613 AUX Inverter, Discontinuous Inductor Current

If the output power is very low ( $\leq 250 \mathrm{~mW}$ ), discontinuous current is preferred for simple loop compensation and freedom from duty-cycle restrictions on the inverter input-output ratio. To ensure discontinuous operation, the inductor must have a sufficiently low inductance to fully discharge on each cycle. This occurs when:
$\mathrm{L}<\left[\mathrm{V}_{\mathrm{IN}} /(\mathrm{IVOUTI}+\mathrm{VIN})\right]^{2}$ RLOAD / (2fAUX) A disconti-nuous-current inverter has a single pole at:

$$
f p=2 /(2 \pi \text { RLOAD COUT })
$$

A type 2 compensation is recommended as shown in Figure 6 except that the RBIAS resistor is connected to REF for the inverter and the reference voltage at the error amplifier is OV .
The crossover frequency for the inverter loop is given by:

$$
\begin{aligned}
& \mathrm{C} 1=[1 /(2 \pi \times \mathrm{fC} \times \mathrm{R} 1)]\left[\mathrm{V}_{\mathrm{IN}} / \mathrm{V}_{\mathrm{RAMP}}\right]\left[\mathrm{R}_{\mathrm{LOAD}} /\right. \\
& \text { ( } \left.2 \mathrm{~L} \mathrm{f}_{\mathrm{AUX}} \text { ) }\right]^{1 / 2}\left[\mathrm{~V}_{\text {REF }} /\left(\text { IVOUT } \mathrm{I}+\mathrm{V}_{\text {REF }}\right)\right]
\end{aligned}
$$

where $\mathrm{V}_{\text {RAMP }}$ is the internal slope-compensation voltage ramp of 1.25 V .
The frequency of the pole and zero are defined by the equations below. R2 and C1 introduce a zero at a frequency given by:

$$
\mathrm{fz}=1 /(2 \pi \mathrm{R} 2 \mathrm{C} 1)
$$

While a pole is introduced at the frequency:

$$
f P 2=1 /(2 \pi R 2 C 2)
$$

The following is a typical procedure for selecting the compensation components for a discontinuous-con-duction-mode inverter:

1) Choose the compensation so the unity-gain crossover, f , occurs at $\mathrm{f}_{\mathrm{A}} \mathrm{X} / \mathrm{I} / 10$ or lower.
2) Set the resistor-divider formed by $R_{1}$ and RBIAS to set the desired output regulation voltage as specified in the Setting Output Voltages section.

R1 = RBIAS (|VOUTI / 1.25) where RBIAS is chosen to be $100 \mathrm{k} \Omega$ or lower.
Note that RBIAS only sets the DC operating point of the loop and has no effect on the AC characteristics.
3) Set the zero fz formed by R2 and C1 to cancel the inverter pole at frequency fp.
4) Set the pole formed by R2 and C2 to cancel the ESR zero of the output capacitor or a decade below the crossover frequency if using ceramic output capacitors

## MAX8612/MAX8613 AUX Inverter, Continuous Inductor Current

 Continuous inductor current may be more suitable for larger load currents (50mA or more). It improves efficiency by lowering the ratio between peak inductor current and output current. It does this at the expense of a larger inductance value that requires larger size for a given current rating. With continuous-inductor-current inverter operation, there is a right-half-plane zero, ZRHP, at:
## 8-Channel PMICs for Digital Camera Power Supplies

$$
Z_{R H P}=\left[(1-D)^{2} / D\right] \times R L O A D /(2 \pi L)
$$

where $\mathrm{D}=\mathrm{IV}$ OUTI $/$ (IVOUTI $+\mathrm{V}_{\text {IN }}$ ) (in an inverter).
There is a complex pole pair at:

$$
f_{0}=(1-D) /\left(2 \pi(L C)^{1 / 2}\right)
$$

If the zero due to the output-capacitor capacitance and ESR is less than $1 / 10$ the right-half-plane zero:

$$
Z_{\text {COUT }}=1 /\left(2 \pi \text { COUT } R_{E S R}\right)<Z_{\text {RHP }} / 10
$$

A type 3 compensation is recommended as shown in Figure 7 except that the RBIAS resistor is connected to REF for the inverter and the reference voltage at the error amplifier is OV. The frequency of the poles and zeros introduced by type 3 compensation network (Figure 7) are defined by the following equations.
The zeros are:

$$
\begin{gathered}
\mathrm{fZ} 1=1 /(2 \pi \mathrm{R} 2 \mathrm{C} 1) \\
\mathrm{fZ} 2=1 /(2 \pi \mathrm{R} 1 \mathrm{C} 3) \text { (assuming } \mathrm{R} 1 \gg \mathrm{R} 3)
\end{gathered}
$$

The poles are:

$$
\begin{gathered}
f P_{1}=1 /(2 \pi \mathrm{R} 3 \mathrm{C} 3) \\
\mathrm{fP}_{2}=1 /(2 \pi \mathrm{R} 2 \mathrm{C} 2)(\text { assuming } \mathrm{C} 1 \gg \mathrm{C} 2)
\end{gathered}
$$

Also, the unity-gain frequency or crossover frequency is:

$$
f_{C}=1 /(2 \pi R 1 C 1)[1 / D(1-D)]
$$

With voltage-mode control the goal of the loop design is to set the crossover frequency above the complex pole pair frequency but below the RHP zero. This is accomplished by placing the two zeros below the complex pole pair as this provides a phase boost. The two poles are then placed a decade above the crossover frequency.
The following is a typical procedure for selecting the compensation components for a continuous-conductionmode inverter:

1) Choose the compensation so the unity-gain crossover, fc , occurs approximately a decade above the complex pole pair but at least before $1 / 6$ the RHP zero frequency and $1 / 10$ the switching frequency fAUX.
2) Set the resistor-divider formed by R1 and RBIAS to set the desired output regulation voltage as specified in the Setting Output Voltages section:
R1 = RBIAS (|VOUT| / 1.25)
where RBIAS is chosen to be $100 \mathrm{k} \Omega$ or lower.
Note that RBIAS only sets the DC operating point of the loop and has no effect on the AC characteristics.
3) Compute C1 knowing the crossover frequency fC and R1.
4) Set the zero fZ2 formed by R1 and C3 approximately halfway between the complex pole pair and the crossover frequency $\mathrm{f}_{\mathrm{C}}$ to compensate for the phase loss.
5) Set the other zero fZ 1 formed by R2 and C1 approximately one-half decade above the complex pole pair.
6) If the zero due to the output capacitance and ESR (ZCOUT $=1 /(2 \pi$ COUT RESR)) is within a decade of the crossover frequency, then set the pole formed by R3 and C3 to cancel the ESR zero. If ZCOUT is much higher than fc (as is typical with ceramic output capacitors) and continuous conduction is required, then set the pole formed by R3 and C3 more than a decade higher than the crossover frequency.
7) Set the second pole formed by R2 and C2 (fp2) more than one-half a decade above the crossover frequency.

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## Applications Information

## Typical Operating Circuits

Figures 1 and 2 show connections for Li+ and 2 AA battery arrangements. Figures 8 and 9 show various connections for the AUX controller.

Figure 1. 2 AA Cell Operation Figure 1 is optimized for $2-$ cell AA inputs ( 1.5 V to 3.6 V ). The SU step-up boost converter generates 5 V from the battery. Likewise, the 3.4 V analog front-end (AFE) supply and 3.3V MAIN logic supplies operate as boost converters (MAX8610/MAX8612) from the battery input. The 1.5 V supply for the DSP core is stepped down from the battery. The -7.5 V for CCD is powered by $\mathrm{V}_{S U}$, the SU converter output. The remaining supplies, +14 V for the CCD, 20mA bias for the white LED backlight, and the supply generated by the AUX boost controller, are all derived directly from the battery.

Figure 2. Li+ Cell or Dual-Battery Operation In the connection in Figure 2, the input voltage range is 3 V to 5 V , covering the operating range of a Li+ battery and $A C$ adapter. Figure 2 will also operate in dual-battery systems that operate from both Li+ and 2 AA cells. The SU step-up supplies 5V. Since boost-buck operation is often needed for the 3.3V MAIN and 3.4V AFE outputs, they are operated as step-down converters (in the MAX8611/MAX8613/MAX8611V) from the SU step-up output (PVSU). By cascading a high-efficiency step-up and step-down converter, boost-buck efficiency reaches $90 \%$ while still providing a regulated output over a wide input voltage range. The SD step-down 1.5V (DSP core) output is powered directly from the battery.


Figure 8. Typical Application for the AUX Boost Controller on the MAX8610/MAX8611/MAX8611V

## AUX Controller Applications

The MAX8610/MAX8611/MAX8611V AUX boost controller can be used for a wide variety of step-up applications. These include generating an additional 5V supply or some other voltage for motor or actuator drive or for generating an additional high-voltage supply. Figure 8 shows an example of an AUX boost application.
On the MAX8612/MAX8613, AUX is set up to drive an external p-channel MOSFET in an inverting configuration. DRVAUX drives low to turn on the MOSFET, and FBAUX has a OV threshold. This is useful for generating a 2nd negative voltage, particularly if more output current is required from the negative supply than can be supplied by the CCD inverter or for the OLED power supply. Figure 9 shows an example circuit.

## Designing a PC Board

Good PC board layout is important to achieve optimal performance from the MAX8610-MAX8613/MAX8611V. Poor design can cause excessive conducted and/or radiated noise. Conductors carrying discontinuous currents and any high-current path should be made as short and wide as possible. A separate low-noise ground plane containing the reference and signal grounds should connect to the power-ground plane at only one point to minimize the effects of power-ground currents. Typically, the ground planes are best connected right at the device. Keep the voltage-feedback network very close to the device, preferably within 0.2in ( 5 mm ) of the FB_ pin. Nodes with high dV/dt (switching nodes) should be kept as small as possible and should be routed away from high-impedance nodes such as FB_. Refer to the MAX8610-MAX8613/MAX8611V EV kit data sheet for a full PC board example.


Figure 9. Typical Application for the AUX Inverting Controller on the MAX8612/MAX8613

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Pin Configuration


Selector Guide

| PART | MAIN AND AFE <br> DC-DC FUNCTION | AUX DC-DC <br> FUNCTION | SKIP <br> LEVELS |
| :--- | :---: | :---: | :---: |
| MAX8610ETM | Boost | Boost | Dual |
| MAX8611ETM | Buck | Boost | Dual |
| MAX8612ETM | Boost | Inverter | Dual |
| MAX8613ETM | Buck | Inverter | Dual |
| MAX8613VETM | Buck | Boost | Single |

Chip Information
TRANSISTOR COUNT: 28,001
PROCESS: BiCMOS

## 8-Channel PMICs for Digital Camera Power Supplies

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)


# 8-Channel PMICs for Digital Camera Power Supplies 

Package Information (continued)
(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)

| COMMON DIMENSIONS |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| PKG. | 36L 6x6 |  |  | 40L 6x6 |  |  | 48L 6x8 |  |  |
| STMBOL | MIN. | NOM. | MAX. | MIN. | NOM. | max. | MiN. | NOM. | max. |
| A | 0.70 | 0.75 | 0.80 | 0.70 | 0.75 | 0.80 | 0.70 | 0.75 | 0.80 |
| A1 | 0 | 0.02 | 0.05 | 0 | 0.02 | 0.05 | 0 | - | 0.05 |
| A2 | 0.20 REF. |  |  | 0.20 REF. |  |  | 0.20 REF. |  |  |
| b | 0.20 | 0.25 | 0.30 | 0.20 | 0.25 | 0.30 | 0.15 | 0.20 | 0.25 |
| D | 5.90 | 6.00 | 6.10 | 5.90 | 6.00 | 6.10 | 5.90 | 6.00 | 6.10 |
| E | 5.90 | 6.00 | 6.10 | 5.90 | 6.00 | 6.10 | 5.90 | 6.00 | 6.10 |
| - | 0.50 BSC. |  |  | 0.50 BSC. |  |  | 0.40 BSC. |  |  |
| k | 0.25 | - | - | 0.25 | - | - | 0.25 | - | - |
| L | 0.45 | 0.55 | 0.65 | 0.30 | 0.40 | 0.50 | 0.30 | 0.40 | 0.50 |
| N | 36 |  |  | 40 |  |  | 48 |  |  |
| ND | 9 |  |  | 10 |  |  | 12 |  |  |
| NE | 9 |  |  | 10 |  |  | 12 |  |  |
| JEDEC | WJJO-1 |  |  | WJJD-2 |  |  | - |  |  |


| EXPOSED PAD VARIATIONS |  |  |  |  |  |  |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: |
| PKG. <br> CODES | D2 |  |  | E2 |  |  |
|  | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| T3666-2 | 3.60 | 3.70 | 3.80 | 3.60 | 3.70 | 3.80 |
| T3666-3 | 3.60 | 3.70 | 3.80 | 3.60 | 3.70 | 3.80 |
| T3666N-1 | 3.60 | 3.70 | 3.80 | 3.60 | 3.70 | 3.80 |
| T3666MN-1 | 3.60 | 3.70 | 3.80 | 3.60 | 3.70 | 3.80 |
| T4066-2 | 4.00 | 4.10 | 4.20 | 4.00 | 4.10 | 4.20 |
| T4066-3 | 4.00 | 4.10 | 4.20 | 4.00 | 4.10 | 4.20 |
| T4066-4 | 4.00 | 4.10 | 4.20 | 4.00 | 4.10 | 4.20 |
| T4066-5 | 4.00 | 4.10 | 4.20 | 4.00 | 4.10 | 4.20 |
| T4866-1 | 4.40 | 4.50 | 4.60 | 4.40 | 4.50 | 4.60 |
| T4866-2 | 4.40 | 4.50 | 4.60 | 4.40 | 4.50 | 4.60 |

NDTES:

1. DIMENSIZNING \& TZLERANCING CZNFIRM TD ASME Y14.5M-1994.
2. ALL DIMENSIDNS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TDTAL NUMBER DF TERMINALS.
4. THE TERMINAL \#1 identifier and terminal numbering canvention shall canform ta JeSd 95-1 SPP-012. dETAILS DF TERMINAL \#1 IDENTIFIER ARE OPTIDNAL, BUT MUST BE LICATED WITHIN THE ZONE INDICATED. THE TERMINAL \#1 IDENTIFIER MAY bE EITHER A MLLD or marked feature.
5. DIMENSIIN b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FRIM TERMINAL TIP.
6. nd and ne refer to the number af terminals an each d and e side respectively.
7. DEPIPULATIDN IS PISSIBLE IN A SYMMETRICAL FASHION.
8. cIPLANARITY applies to the expased heat sink slug as well as the terminals.
9. DRAWING CDNFRRMS TD JEDEC MD220, EXCEPT FIR 0.4 mm LEAD PITCH

PACKAGE T4866-1.
10. WARPAGE SHALL NDT EXCEED 0.10 mm .

亿. marking is for package orientation reference ancy.
HPALLAS /VIMKI/VI
12. NUMBER DF LEADS SHOWN FIR REFERENCE $\quad$ NLLY.

PACKAGE GUTLINE,
36, 40, 48L THIN QFN, $6 \times 6 \times 0.8 \mathrm{~mm}$
-DRAWING NOT TO SCALE-

| 36, 40, 48L THIN QF N, $6 \times 6 \times 0.8 \mathrm{~mm}$ |  |  |
| :--- | :--- | ---: | :---: |
| APPROVAL | DOCUMENT CONTROL NO. |  |
| $21-0141$ | H | $2 / 2$ |

## Revision History

Pages changed at Rev 4: 1, 6, 10, 19, 36, 37

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